

LG

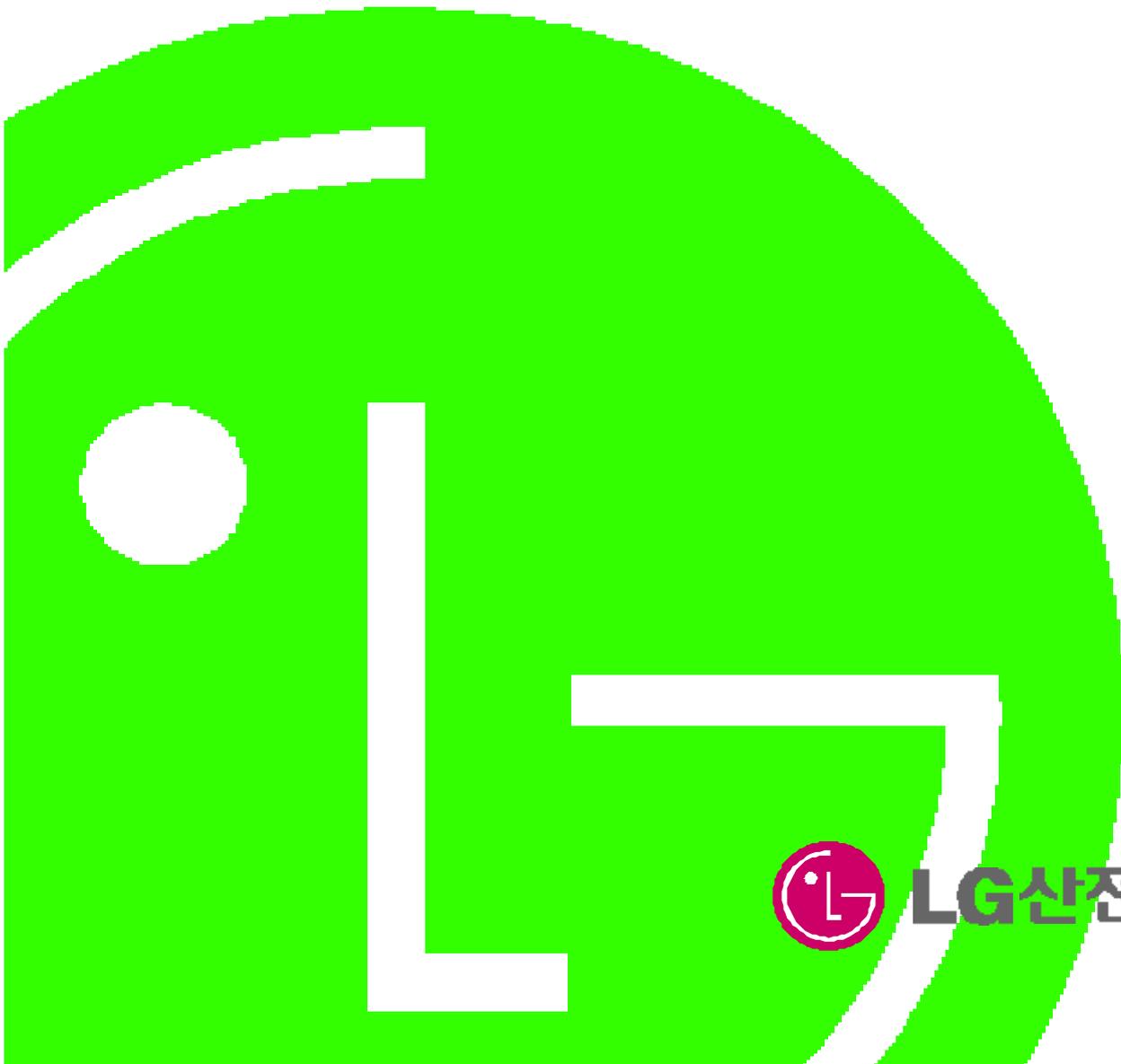
***GLOFA***  
***MASTER-K***

G4F – H01A

G4F – HD1A

G6F – H01A

G6F – HD1A



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7 MK

7.1 / ..... 7-1

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8

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8.2.4 ..... 8-5

A

---

...

2가



가



가



가



가





---

› / 100mm

›

› 가





---

› PLC

›

›

›





---

› FG PLC 3

› PLC

›

›

› 가



Warning symbol (triangle with exclamation mark and lightning bolt)

가

Off

Warning symbol (triangle with exclamation mark and lightning bolt)

PCB

Off

On

Off



Warning symbol (triangle with exclamation mark and lightning bolt)



2002. 9.		

# 1

GLOFA PLC GM4,6 CPU MASTER-K PLC 300S/200S CPU  
GM4 K300S G4F-H01A/G4F-HD1A, GM6 K200S G6F-H01A/G6F-HD1A( ) .

1) 1

(1) 가

(2) B 가

2) 2 1 ,2 ,4 가

3) CW / CCW A B 가

4) (Preset)/ (Gate)

5) 7가

6) , , , , 5  
가 가 .

2.1

GLOFA GM MASTER-K

No.						
1		0 ~ 55				
2		-25 ~ 70				
3		5 ~ 95%RH,				
4		5 ~ 95%RH,				
5					-	X, Y, Z 10 IEC61131-2
			가			
		10 ≤ f < 57Hz	-	0.075mm		
		57 ≤ f ≤ 150Hz	9.8m/s <sup>2</sup> {1G}	-		
			가			
		10 ≤ f < 57Hz	-	0.035mm		
		57 ≤ f ≤ 150Hz	4.9m/s <sup>2</sup> {0.5G}	-		
6		<ul style="list-style-type: none"> <li>가 : 147 m/s<sup>2</sup>{15G}</li> <li>가 : 11ms</li> <li>: (X, Y, Z 3 3 )</li> </ul>				IEC61131-2
7		± 1,500 V				LG
		: 4kV ( )				IEC61131-2 IEC1000-4-2
		27 ~ 500 MHz, 10 V/m				IEC61131-2, IEC1000-4-3
		/		(24V )	(24V )	IEC61131-2 IEC1000-4-4
		2kV	1kV	0.25kV		
8		가 , 가				
9		2,000m				
10		2				
11						

1) IEC(International Electrotechnical Commission : )  
 : 가  
 2)  
 : 2 ,

2.2

2.2.1

		G4F-H01A	G6F-H01A	G4F-HD1A	G6F-HD1A
		64			
		2			
		A , B			
		DC5/12/24V		RS-422A Line Drive	
		Open Collector		Line Driver	
		-2,147,483,648 ~ 2,147,483,647 ( 32 )			
		200 KHz		500 KHz	
가/	1	B			
	2				
	CW/CCW	A : 가			
		B :			
	Out 0 Out 1 Out 2 Out 3 (>, =, <, )				
	( , 10 ~ 30V)				
		DC 5V / 12V / 24V			
	1	1 / 2 ( )			
	2	1 / 2 / 4 ( )			
가		Clear, Latch, ,			
		400mA	450mA	400mA	450mA
		173 g	126g	184 g	134 g

## 2.2.2

ON	DC 5 V	4.5 V	EIA RS-422A Line Driver
	DC 12 V	11 V	
	DC 24 V	14 V	
OFF	DC 5 V	0.8 V	
	DC 12 V	1.5 V	
	DC 24 V	2.5 V	

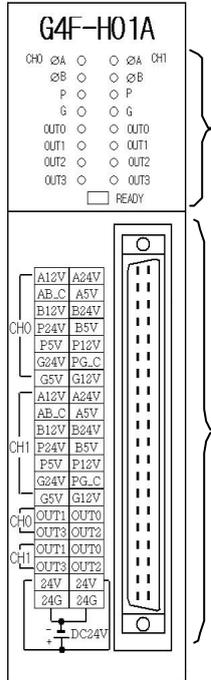
## 2.2.3

	DC 5V / 12V / 24V	
On	DC 5V	DC 4.5V
	DC 12V	DC 11V
	DC 24V	DC 14V
Off	DC 5V	DC 0.8V
	DC 12V	DC 1.5V
	DC 24V	DC 2.5V
On	1ms	
Off	1ms	
	DC 24V, 100 mA/	
	0.1 mA	
	2.5 V	
On	0.1 ms	
Off	0.1 ms	

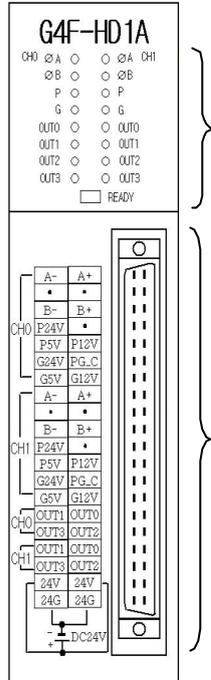
2.3

2.3.1

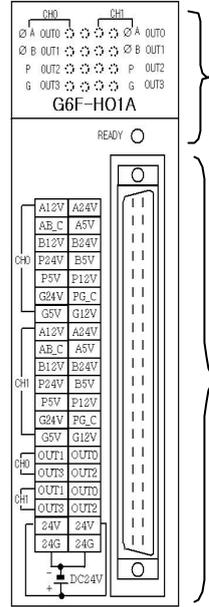
1) G4F-H01A



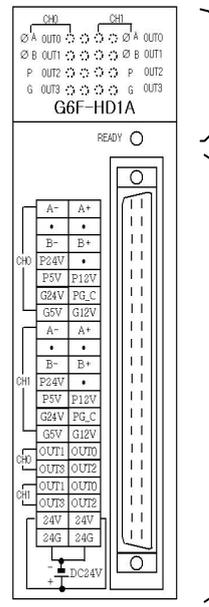
2) G4F-HD1A



3) G6F-H01A



4) G6F-HD1A



	LED	ØA	A
		ØB	B
		P	
		G	
		OUT0	OUT0
		OUT1	OUT1
		OUT2	OUT2
		OUT3	OUT3
		READY	Ready

2.3.2

1)

(1) G4F-H01A/G6F-H01A

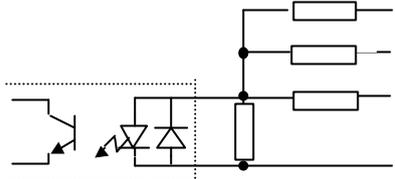
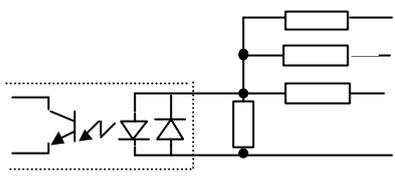
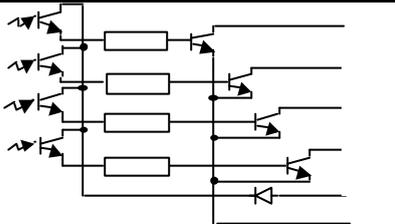
		CH0	CH1		
	1	15	A12V	A	DC12V
	2	16	A24V	A	DC24V
	3	17	AB_C	A/B	COM
	4	18	A5V	A	DC5V
	5	19	B12V	B	DC12V
	6	20	B24V	B	DC24V
	7	21	P24V		DC24V
	8	22	B5V	B	DC5V
	9	23	P5V		DC5V
	10	24	P12V		DC12V
	11	25	G24V		DC24V
	12	26	PG_C	/	COM
	13	27	G5V		DC5V
	14	28	G12V		DC12V
29	33	OUT1		OUT1	
30	34	OUT0		OUT0	
31	35	OUT3		OUT3	
32	36	OUT2		OUT2	
37	38	24V		DC24V	
39	40	24G			

(2) G4F-HD1A/G6F-HD1A

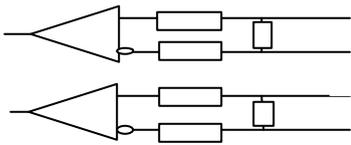
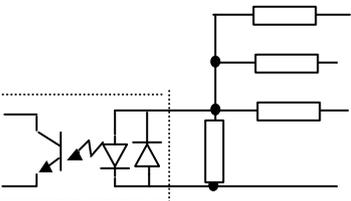
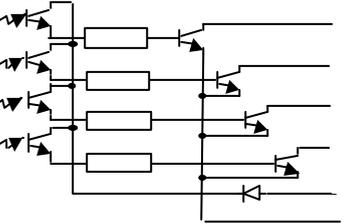
		CH0	CH1		
	1	15	A-	A-	
	2	16	A+	A+	
	3	17	-	-	
	4	18	-	-	
	5	19	B-	B-	
	6	20	B+	B+	
	7	21	P24V		DC24V
	8	22	-	-	
	9	23	P5V		DC5V
	10	24	P12V		DC12V
	11	25	G24V		DC24V
	12	26	PG_C	/	COM
	13	27	G5V		DC5V
	14	28	G12V		DC12V
29	33	OUT1		OUT1	
30	34	OUT0		OUT0	
31	35	OUT3		OUT3	
32	36	OUT2		OUT2	
37	38	24V		DC24V	
39	40	24G			

2)

(1) G4F-H01A/ G6F-H01A

				Ch0	Ch1		
	A24V	2	16	A	24V		
	A12V	1	15	A	12V		
	A5V	4	18	A	5V		
	AB_COM	3	17	A/B	Common		
	B24V	6	20	B	24V		
	B12V	5	19	B	12V		
	B5V	8	22	B	5V		
	P24V	7	21		24V		
	P12V	10	24		12V		
	P5V	9	23		5V		
	PG_COM	12	26	/	Common		
	G24V	11	25		24V		
	G12V	14	28		12V		
	G5V	13	27		5V		
							
OUT0	30	34		0			
OUT1	29	33		1			
OUT2	32	36		2			
OUT3	31	35		3			
24V	37	38		24V			
24G	39	40		Ground			

(2) G4F-HD1A/ G6F-HD1A

				Ch0	Ch1		
	A+	2	16	A+			
	A-	1	15	A-			
	B+	6	20	B+			
	B-	5	19	B-			
	P24V	7	21		24V		
	P12V	10	24		12V		
	P5V	9	23		5V		
	PG_COM	12	26	/	Common		
	G24V	11	25		24V		
	G12V	14	28		12V		
	G5V	13	27		5V		
	OUT0	30	34		0		
	OUT1	29	33		1		
	OUT2	32	36		2		
	OUT3	31	35		3		
	24V	37	38		24V		
	24G	39	40		Ground		

2.4

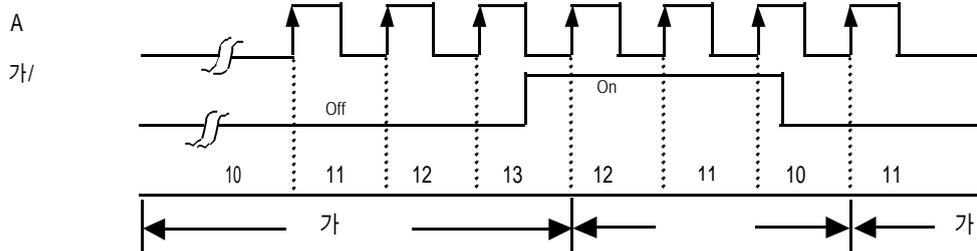
CPU (CTU,CTD,CTUD )  
 32 (-2,147,483,648 ~ 2,147,483,647)  
 1 2 CW/ CCW  
 가/  
 1) 1 : (1) 가/  
 (2)B 가/  
 2) 2 : A B  
 3) CW/CCW : A B LOW 가 , B A LOW  
 가

2.4.1

1) 1  
 (1) 가/ 가

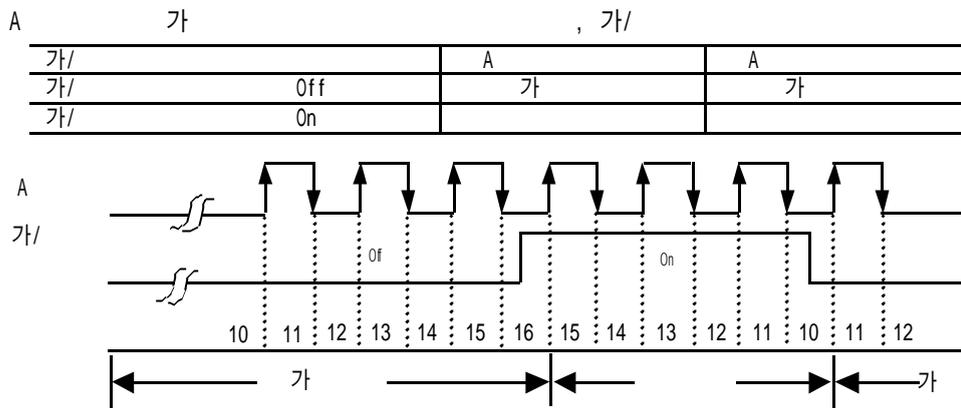
가)1 1 1

A	가	, 가/
가/	A	A
가/	Off	가
가/	On	-



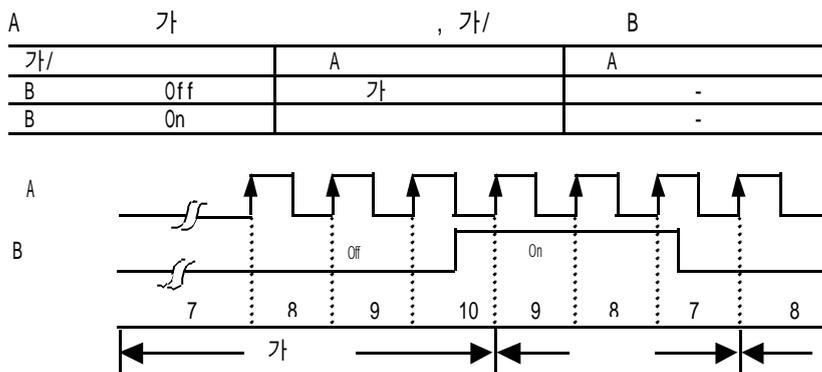
On

)1 1 2

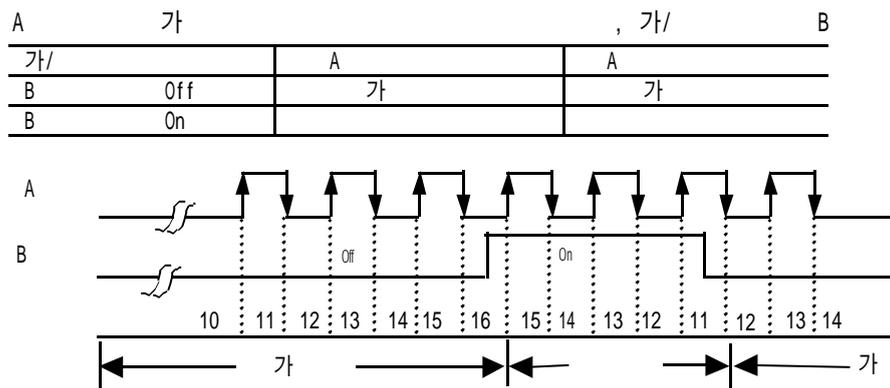


(2) B 가/ 가

가) 1 2 1



)1 2 2

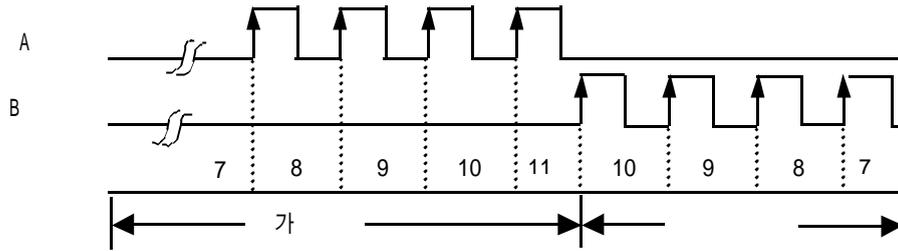




3) CW(Clockwise)/CCW(Counter Clockwise)

A            가            ,            B            가            ,  
 B            가 Low            A            가            ,  
 A            가 Low            B

가/	A            High	A            Low
B            High	-	
B            Low	가	-



2.4.2

	2		MASTER-K		
	GLOFA		0	1	1 33
(Linear)	HSCB_MOD	SEL			
(Ring)	" 0 "				
	" 1 "				

1) (Linear)

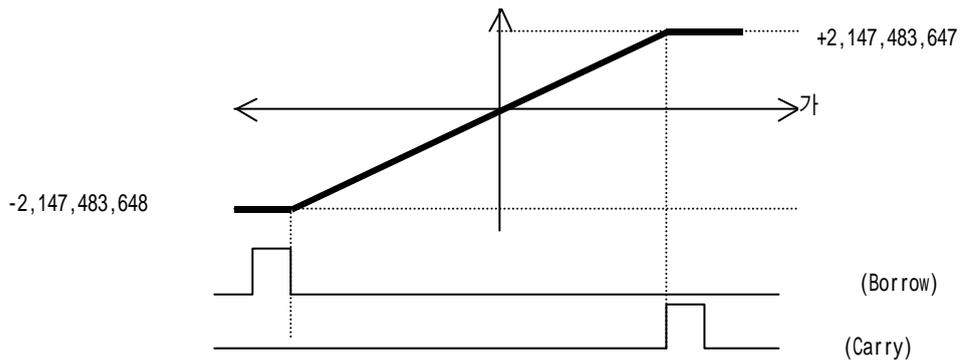
(Linear) : -2,147,483,648 ~ 2,147,483,647

가 , (Carry)가 ,

(Borrow)가 .

(Carry)가 , 가 가 .

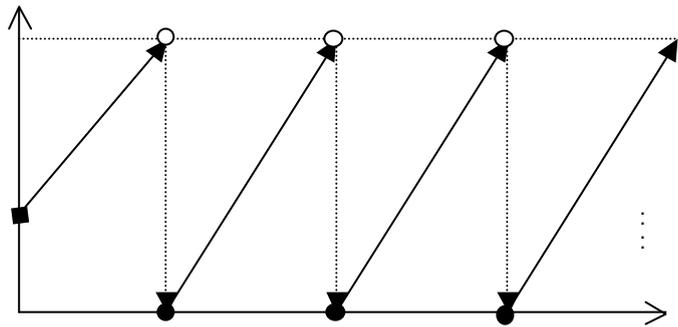
(Borrow)가 , 가 가 .



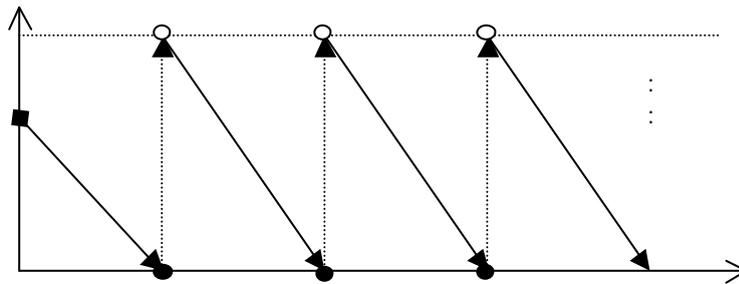
2) (Ring)

(Ring) : ~ Ring  
 : (Ring)

(1) 가  
 가 (Carry)  
 (Linear)



(2)  
 (Borrow)  
 (Linear)



(3) (Ring) (가 )

(Ring)

- 가 2,147,483,647 가  
 ( 2,147,483,648 ) , (Carry) 가



2.4.3

4 가 ,  
>, = , < 7가

	GLOFA	MASTER-K	
	HSCB_CMP CMPS	0	1
		Out0	3
	Out1	4	36
	Out2	5	37
	Out3	6	38
<	" 0 "	" 0 "	
	" 1 "	" 1 "	
=	" 2 "	" 2 "	
	" 3 "	" 3 "	
>	" 4 "	" 4 "	
1 2	" 5 "	" 5 "	
1 , 2	" 6 "	" 6 "	

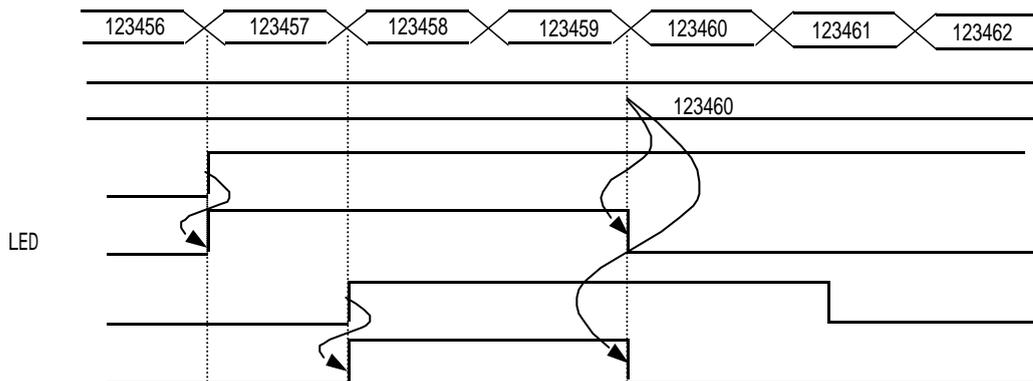
On ( ,  
LED ), On .

	GLOFA	MASTER-K
(LED )	HSCB_OUT CMP_E " 1 "	0 P(n+2)4, 1 P(n+3)4 " On "
( )	HSCB_OUT OUT_E " 1 "	0 P(n+2)5, 1 P(n+3)5 " On "
	HSCB_OUT EQ0_R ~ EQ3_R " 1 " (4 )	0 P(n+2)6 ~ P(n+2)9, 1 P(n+3)6 ~ P(n+3)9 " On " (4 )

LED가 , 가

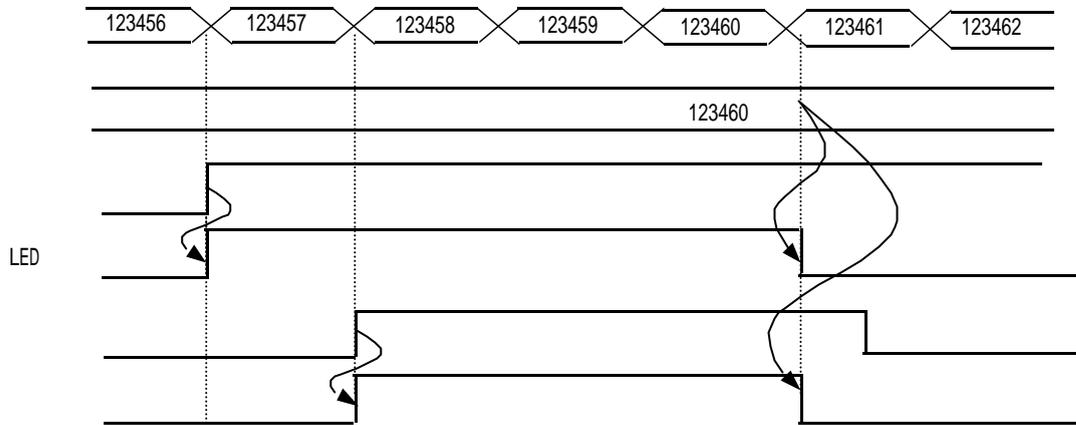
1) 0 ( < )

가 ,



2) 1 ( )

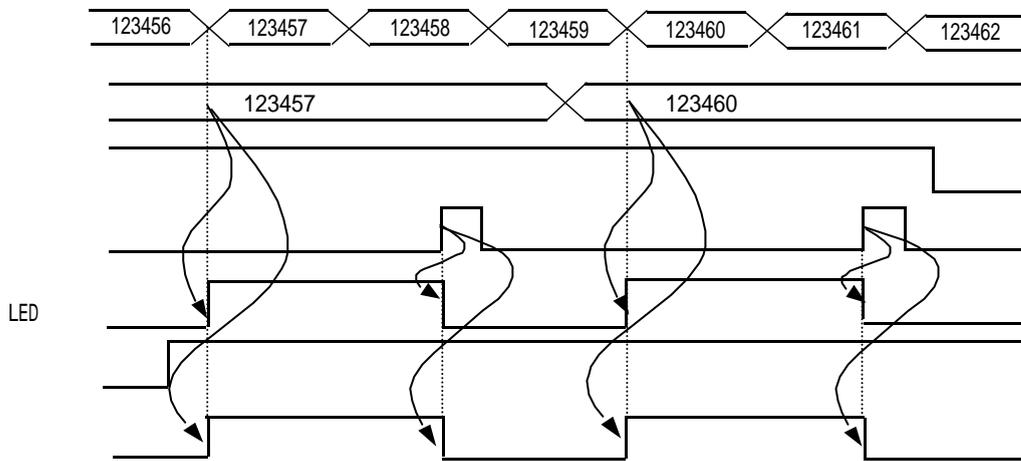
가 ,



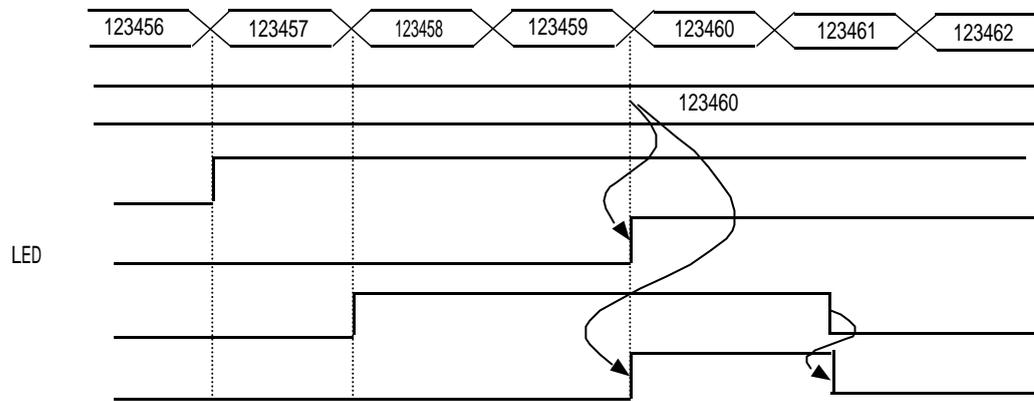
3) 2 ( = )

가 ,

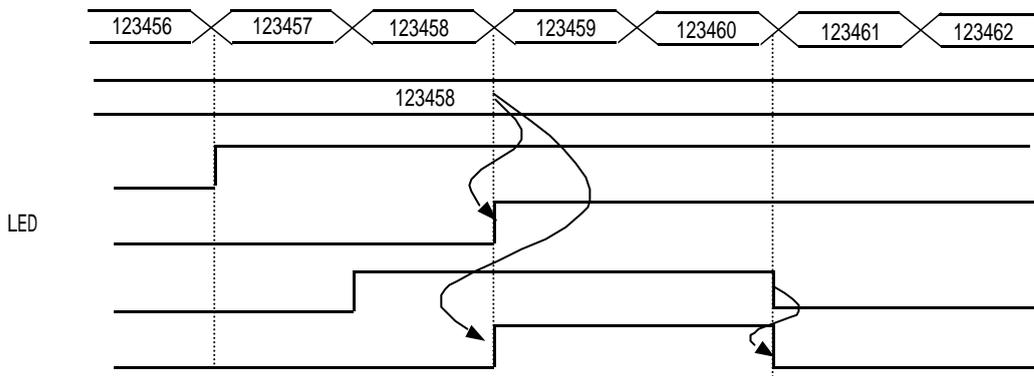
On  
Off (EQ0R ~ EQ3R) On



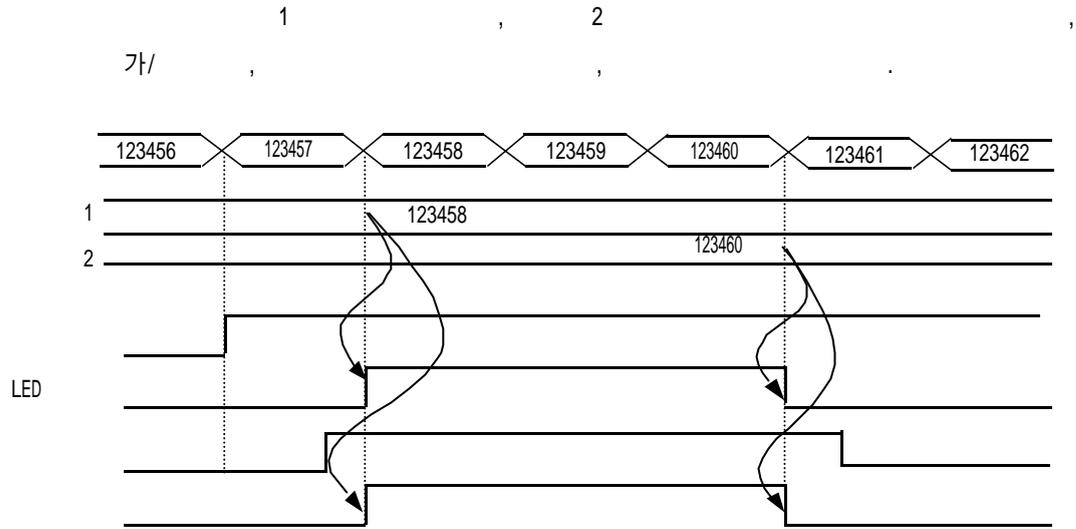
4) 3 ( )



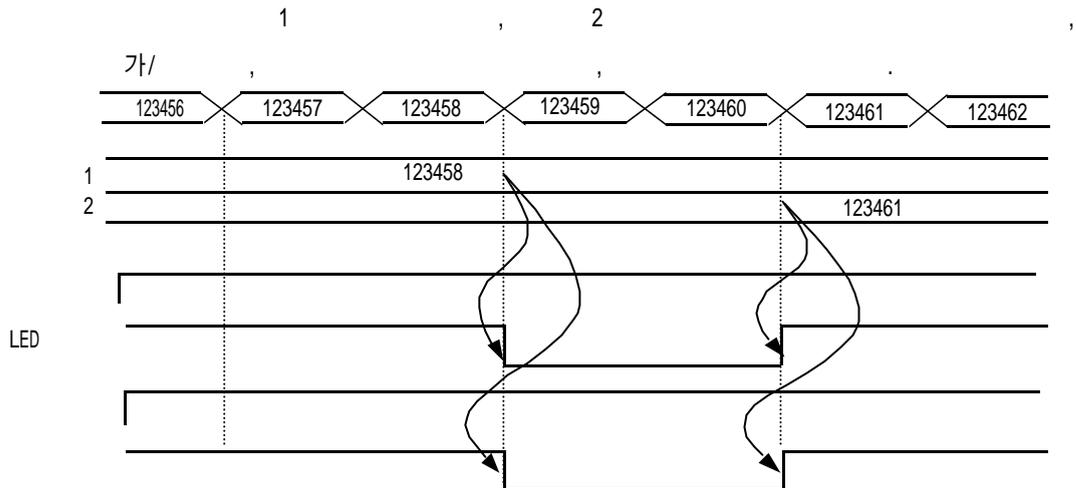
5) 4 ( > )



6) 5 ( 1 2)



7) 6 ( 1, 2)



2.4.4 (Carry)

(Carry) 가

1) (Linear) , 2,147,483,647 .

2) (Ring) , (Ring) .

(Carry)

1) (Linear) , (Carry)가 .

2) (Ring) , (Carry)가 , .

(Carry)

- (Carry) / (Carry/Borrow) On .

GLOFA		MASTER-K		
HSCB_WR	CY_R	0	P(n+2)A	" 0n "
" 1 "		1	P(n+3)A	" 0n "

2.4.5 (Borrow)

(Borrow) 가

- (Linear) , -2,147,483,648 .

- (Ring) , ring .

(Borrow)

- (Linear) , (Borrow)가 .

- (Ring) , (Borrow) , .

(Borrow)

- (Borrow) / (Carry/Borrow) (HSCB\_WR CY\_R) On

GLOFA		MASTER-K		
HSCB_WR	CY_R	0	P(n+2)A	" 0n "
" 1 "		1	P(n+3)A	" 0n "

2.4.6 가

가 가

		GLOFA		MASTER-K	
가		HSCB_WR	0	P(n+2)3	"0n"
		AUX_E "1"	1	P(n+3)3	"0n"
가	Clear	-	-		
	Latch	HSCB_CNT LTCH_OLD	0 : 66, 67 1 : 82, 83		
		HSCB_CNT SCNT_NEW	0 : 68, 69 1 : 84, 85		
		HSCB_AUX AUX	0 2 1 34	A 0 : 70, 71 1 : 86, 87 B 0 : 72, 73 1 : 88, 89	
		HSCB_CNT SCNT_NEW LTCH_OLD	0 : 66, 67 1 : 82, 83 0 : 68, 69 1 : 84, 85		

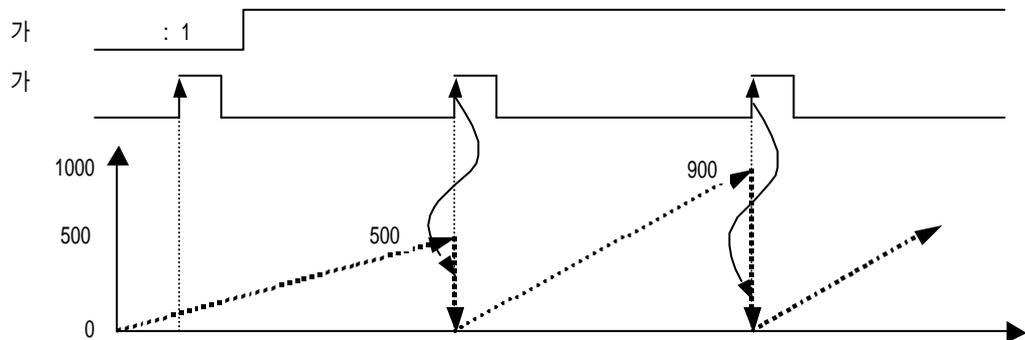
1)

가 (HSCB\_WR AUX\_E) 가 0n , 0

- 가 (HSCB\_AUX AUX) 1 -> 가 On.

Clear 가 가 On

가 가 On

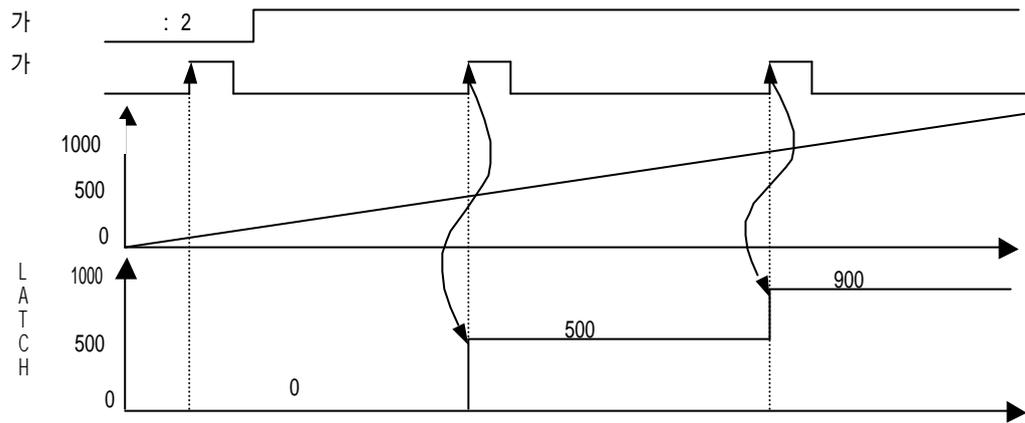


2)

가 가 On , Latch .

- 가 2 -> 가 On .  
 가 가 On . , 가

가 On .  
 가 가 On , (HSCB\_CNT) LTCH\_OLD



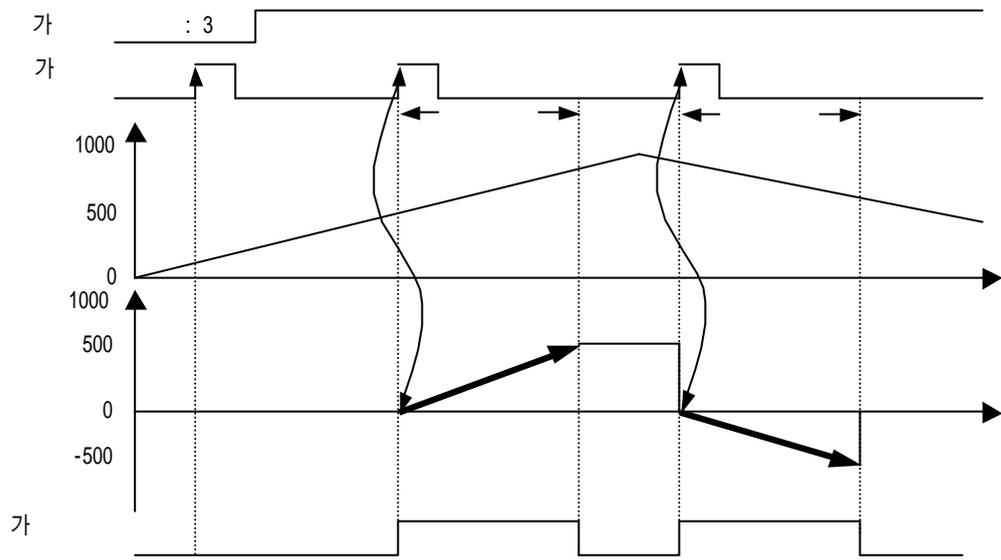
3)

가 가 0n , .

- 가 3 -> -> 가 0n. 0  
 가 가 0n  
 . , 가 가 0n .  
 (HSCB\_CNT) SCNT\_NEW .

가

- 가 가 0n , 가  
 (HSCB\_RD AUX\_ING) 가 0n .



4)

가 가 On , .

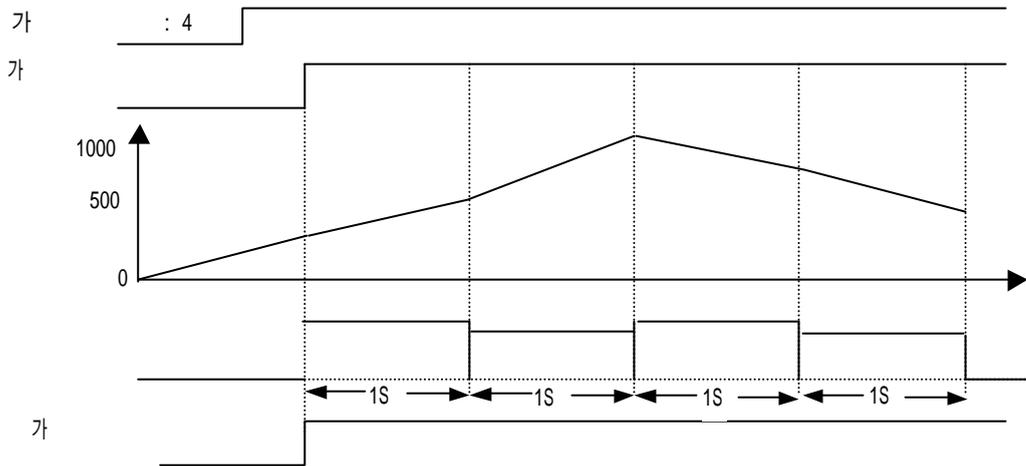
- 가 4 -> 가 On.

가 가 On (HSCB\_CNT TIME\_A/  
TIME\_B (A B )).

- 
$$= \frac{25,000,000}{T} \quad T :$$

가

- 가 가 On , 가  
(HSCB\_RD AUX\_ING) 가 On .



5)

가 가 On

- 가 5 -> -> 가 On.  
가 가 On

(HSCB\_CNT) SCNT\_NEW LTCH\_OLD

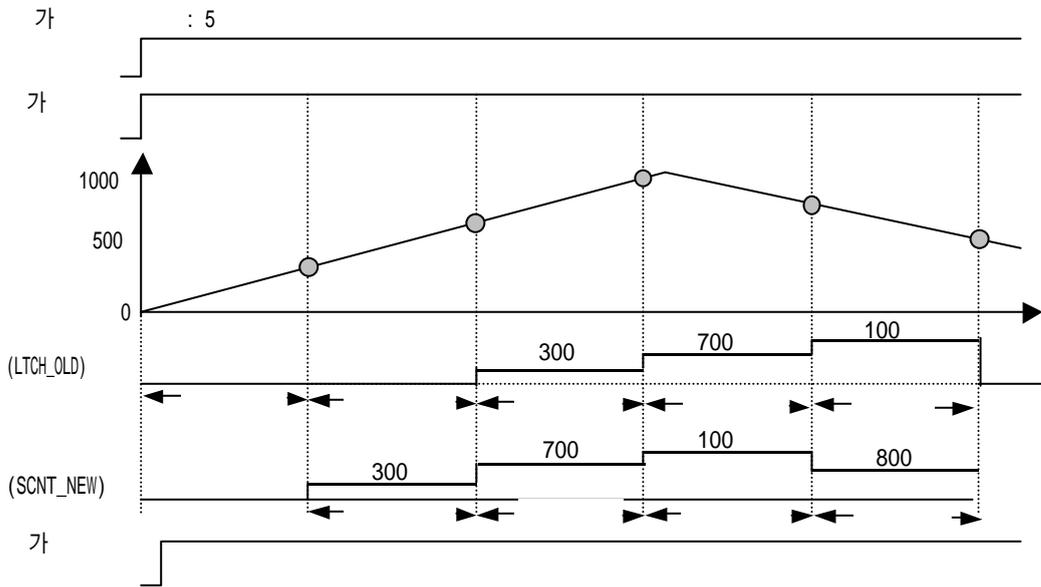
- (PPU) = SCNT\_NEW LTCH\_OLD  
1 (60000ms) (RPM)

- RPM ( ) =  $\frac{PPU}{P}$

PPU : , P : 1

가

- 가 가 On  
가 (HSCB\_RD AUX\_ING) 가 On



3.1

3.1.1

가

1)

- 가
- 가
- 
- 
- 가 0-55

2)

- 가 PLC 가 가
- 
- 
- 50mm
- 

3.1.2

1)

2)

PCB

3)

가

4)

3.2

1)

3

2)

3)

1

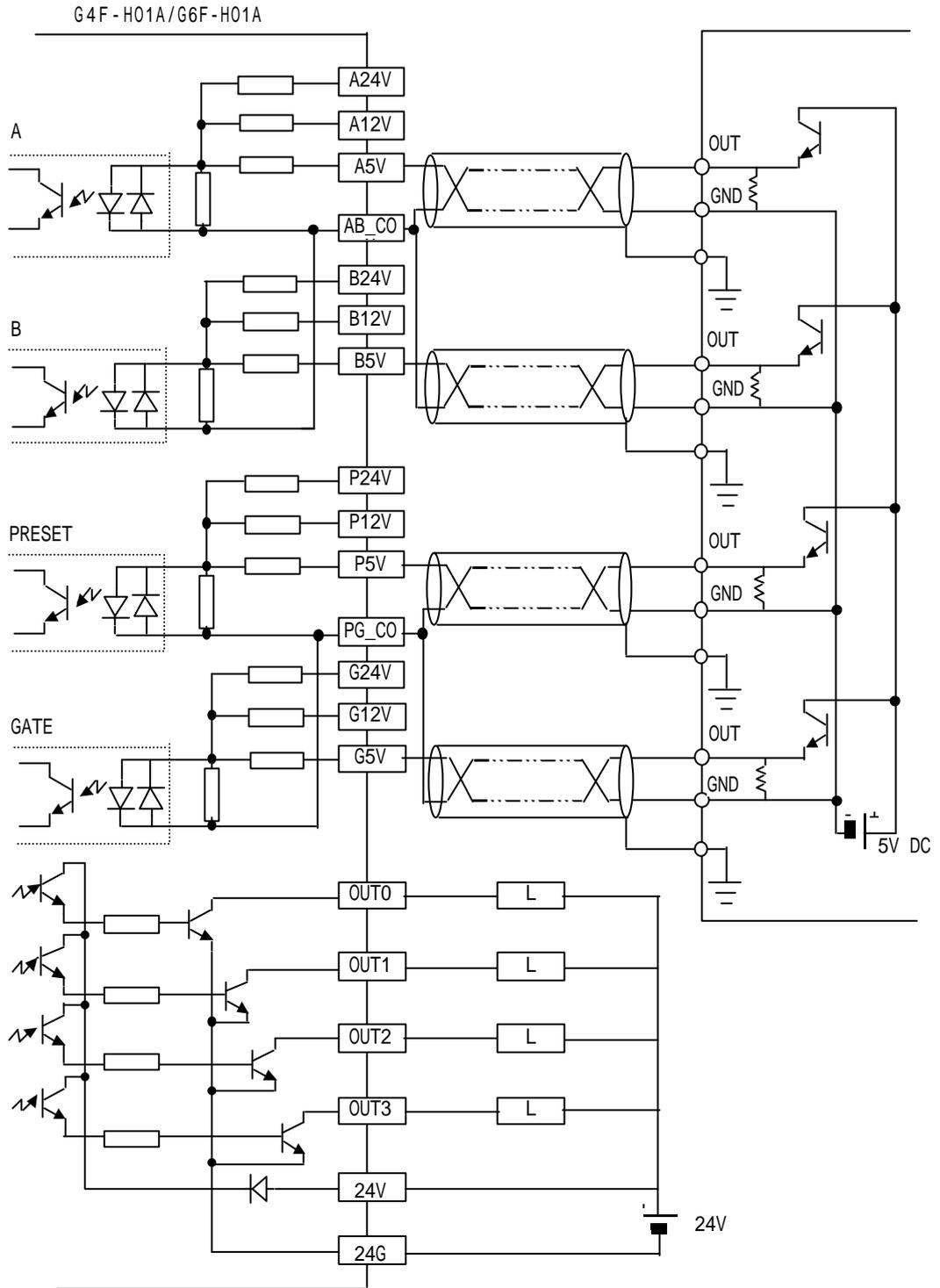
A

2

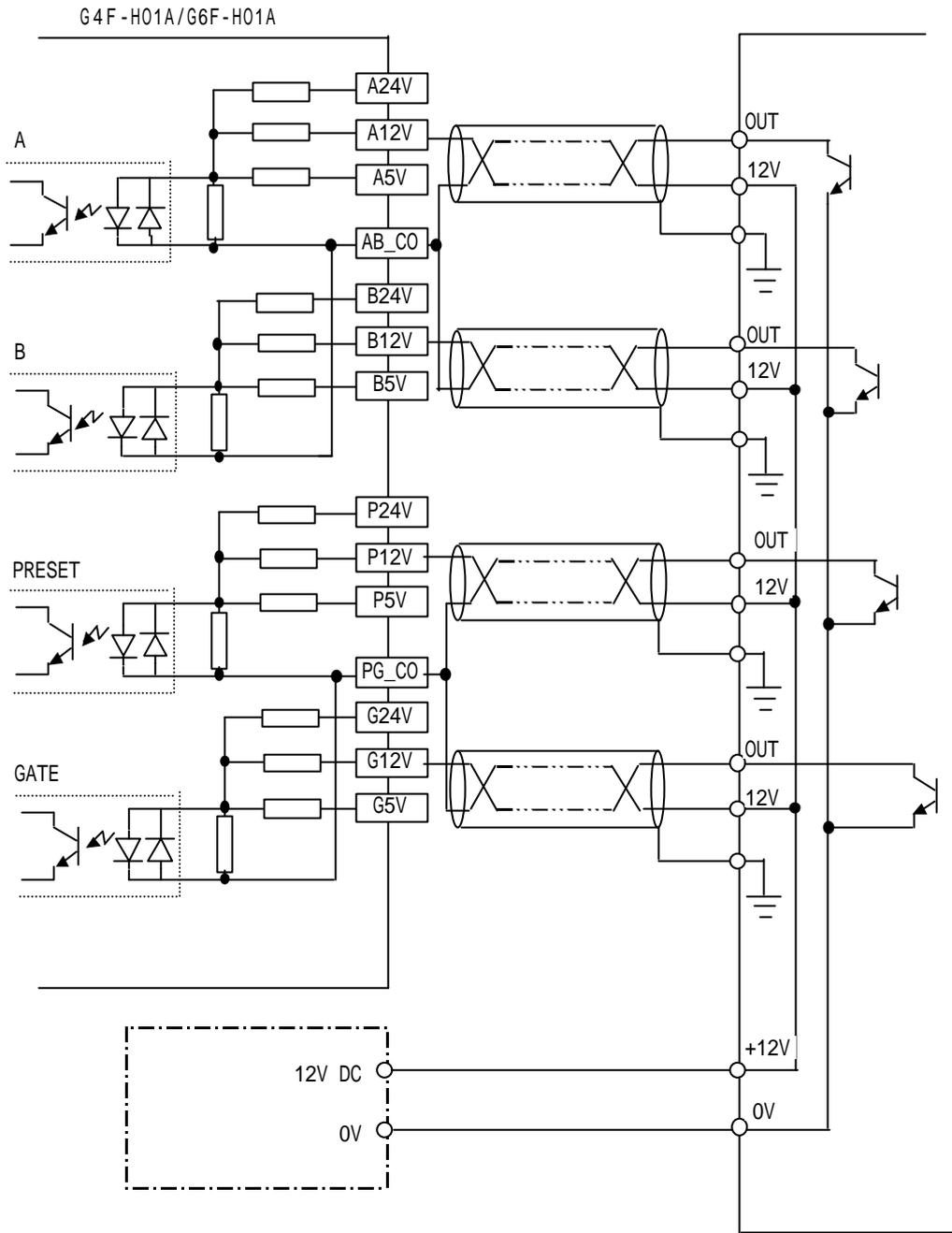
A , B

3.2.1 DC5V

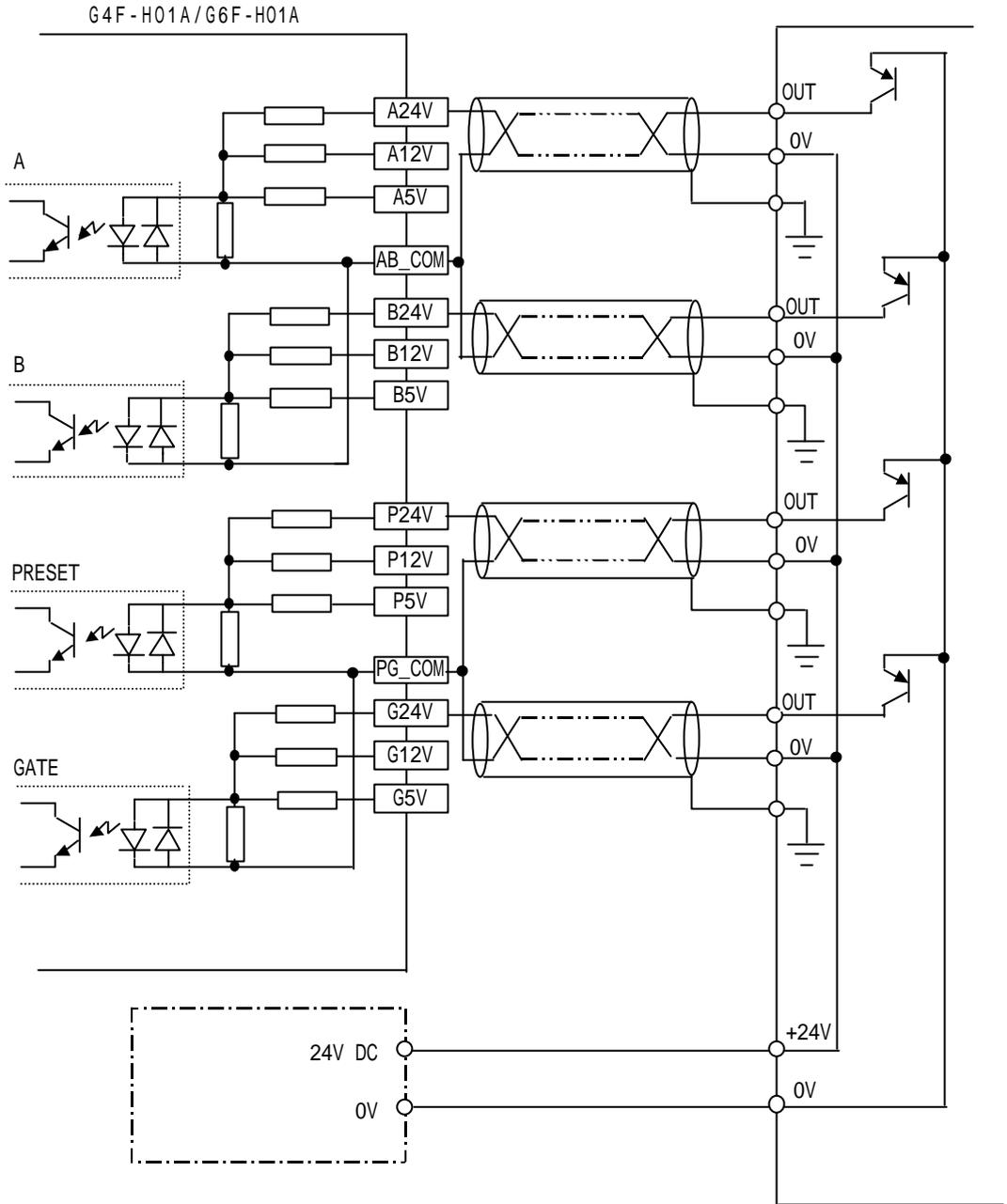
- 가
- 가
- 



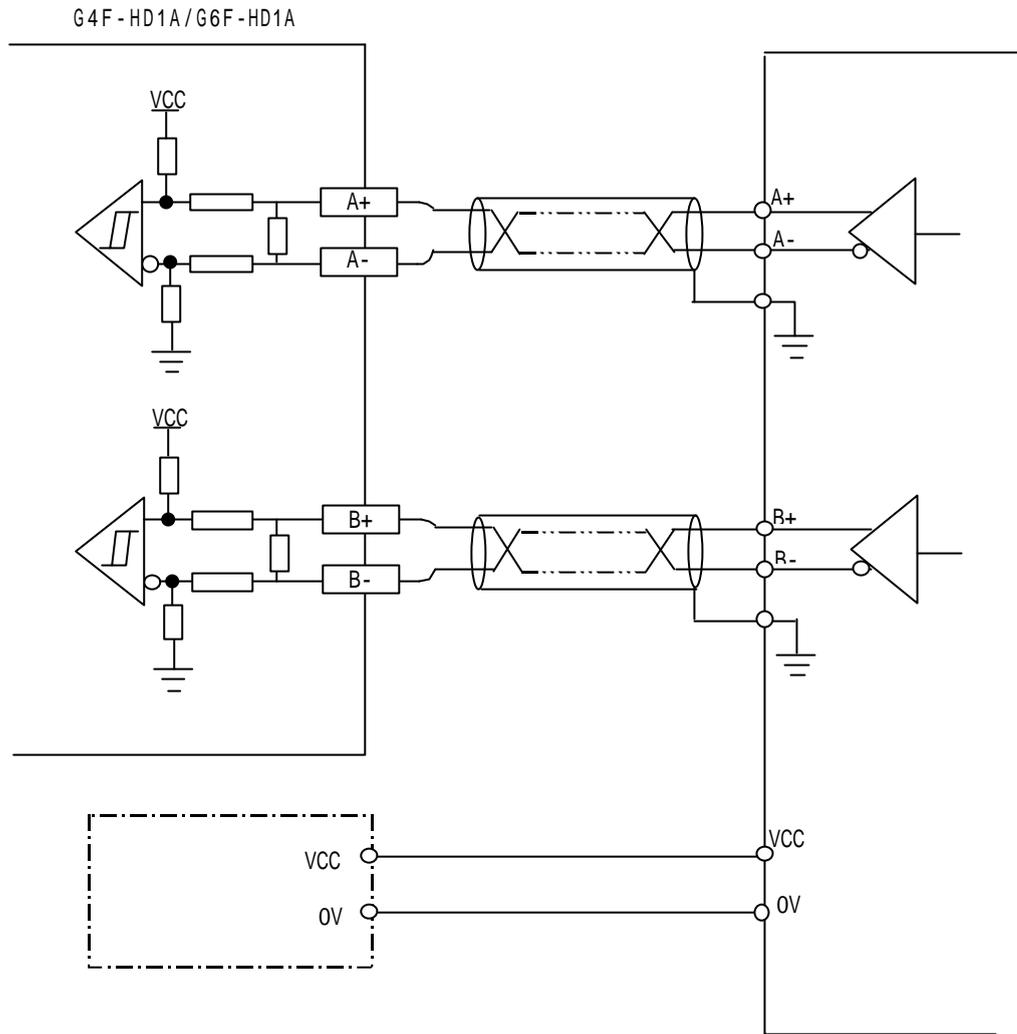
3.2.2 DC12V NPN



3.2.3 DC24V PNP



3.2.4



4

GMWIN

No	G4F-H01A		G6F-H01A		
	G4F-HD1A		G6F-HD1A		
1	HSCB_PRE	HSCBRPRE	HSCB_PRE	HSCBRPRE	(Preset)
2	HSCB_MOD	HSCBRMOD	HSCB_MOD	HSCBRMOD	
3	HSCB_AUX	HSCBRAUX	HSCB_AUX	HSCBRAUX	가
4	HSCB_CMP	HSCBRCMP	HSCB_CMP	HSCBRCMP	
5	HSCB_CNT	HSCBRCNT	HSCB_CNT	HSCBRCNT	
6	HSCB_WR	HSCBRWR	HSCB_WR	HSCBRWR	
7	HSCB_RD	HSCBRRD	HSCB_RD	HSCBRRD	
8	HSCB_OUT	HSCBROUT	HSCB_OUT	HSCBROUT	

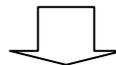
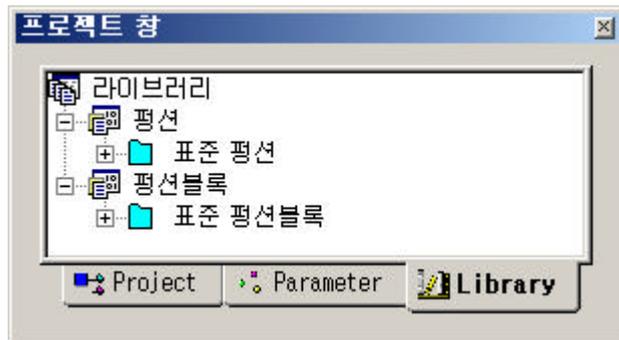
4.1 GMWIN

GMWIN

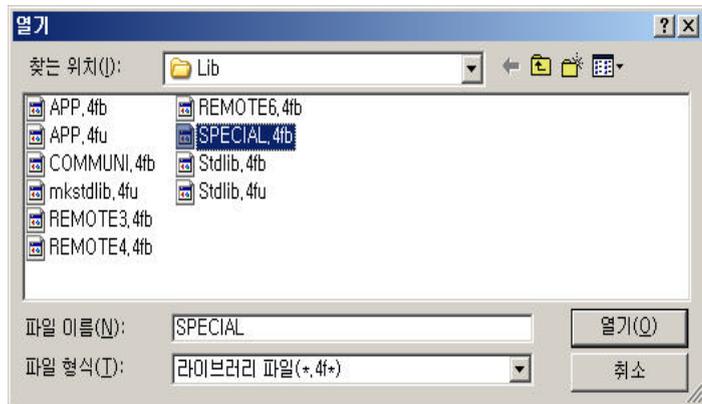
가 가



- |                     |
|---------------------|
| G4F-H01A , G4F-HD1A |
| 1. Special.4fb      |
| 2. Remote3.4fb      |
| 3. Remote4.4fb      |
| G6F-H01A , G6F-HD1A |
| 1. Special.6fb      |
| 2. Remote3.6fb      |
| 3. Remote4.6fb      |
| 4. Remote6.6fb      |



GMWIN V4.0



4.2

4.2.1

(HSCB\_PRE)

		Datatype	
<div style="border: 1px solid black; padding: 2px; width: fit-content;">                     HSCB_PRE                      - REQ DONE                      - BASE STAT                      - SLOT                      - CH                      - PSET                 </div>	REQ	BOOL	(Preset) "0 1"
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )
	SLOT	USINT	: 0 7
	CH	BOOL	"0" 0 , "1" 1
	PSET	DINT	: -2,147,483,648 2,147,483,647
	DONE	BOOL	(Preset) "1" , 가 "0" "1" ,
	STAT	USINT	(Preset) 가

4.2.2

(HSCB\_MOD)

		Datatype																	
<div style="border: 1px solid black; padding: 2px;">                     HSCB_MOD                      └─ REQ DONE                      └─ BASE STAT                      └─ SLOT                      └─ CH                      └─ MODE                      └─ SEL                      └─ RING_L                      └─ RING_H                 </div>	REQ	BOOL	"0 1"																
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )																
	SLOT	USINT	: 0 7																
	CH	BOOL	"0" 0 , "1" 1																
	MODE	USINT	: 0 7 <table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0</td><td>2 1</td></tr> <tr><td>1</td><td>2 2</td></tr> <tr><td>2</td><td>2 4</td></tr> <tr><td>3</td><td>CW/CCW</td></tr> <tr><td>4</td><td>1 1 1 ( 가 )</td></tr> <tr><td>5</td><td>1 1 2 ( 가 )</td></tr> <tr><td>6</td><td>1 2 1 (B 가 )</td></tr> <tr><td>7</td><td>1 2 2 (B 가 )</td></tr> </table>	0	2 1	1	2 2	2	2 4	3	CW/CCW	4	1 1 1 ( 가 )	5	1 1 2 ( 가 )	6	1 2 1 (B 가 )	7	1 2 2 (B 가 )
	0	2 1																	
	1	2 2																	
	2	2 4																	
	3	CW/CCW																	
	4	1 1 1 ( 가 )																	
	5	1 1 2 ( 가 )																	
	6	1 2 1 (B 가 )																	
7	1 2 2 (B 가 )																		
SEL	BOOL	0 : Linear 1 : Ring																	
RING_L	DINT	Ring : -2,147,483,648 2,147,483,647																	
RING_H	DINT	Ring : -2,147,483,648 2,147,483,647																	
DONE	BOOL	"1" , 가 "0" , "1" ,																	
STAT	USINT	가																	

4.2.3 가 (HSCB\_AUX) 가

		Datatype													
<div style="border: 1px solid black; padding: 5px; width: fit-content;">                     HSCB_AUX                      REQ DONE                      BASE STAT                      SLOT                      CH                      AUX                      SET_TIME                 </div>	REQ	BOOL	가 "0 1"												
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )												
	SLOT	USINT	: 0 7												
	CH	BOOL	"0" 0 , "1" 1												
	AUX	USINT	가 : 0 5 <table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0</td><td>가</td></tr> <tr><td>1</td><td></td></tr> <tr><td>2</td><td></td></tr> <tr><td>3</td><td></td></tr> <tr><td>4</td><td></td></tr> <tr><td>5</td><td></td></tr> </table>	0	가	1		2		3		4		5	
	0	가													
	1														
	2														
	3														
	4														
5															
SET_TIME	UINT	: 1 65,535 (ms)													
		: 1 65,535 (ms)													
DONE	BOOL	가 "1" , 가 "0" , "1"													
STAT	USINT	가 가													

4.2.4

(HSCB\_CMP)

/

		Datatype																						
<div style="border: 1px solid black; padding: 2px; width: fit-content;">                     HSCB_CMP                      REQ    DONE                      BASE    STAT                      SLOT                      CH                      CMPS                      CMPL                      CMPH                 </div>	REQ	BOOL	"0" 1																					
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )																					
	SLOT	USINT	: 0 7																					
	CH	BOOL	"0" 0 , "1" 1																					
	CMPS	USINT [Array] *1	: 0 6 <table border="1" style="margin-left: 20px;"> <tr><td>0</td><td>&lt;</td><td>:</td></tr> <tr><td>1</td><td></td><td>:</td></tr> <tr><td>2</td><td>=</td><td>:</td></tr> <tr><td>3</td><td></td><td>:</td></tr> <tr><td>4</td><td>&gt;</td><td>:</td></tr> <tr><td>5</td><td></td><td>:</td></tr> <tr><td>6</td><td></td><td>:</td></tr> </table>	0	<	:	1		:	2	=	:	3		:	4	>	:	5		:	6		:
	0	<	:																					
	1		:																					
	2	=	:																					
	3		:																					
4	>	:																						
5		:																						
6		:																						
CMPL	DINT [Array] *1	: -2,147,483,648 2,147,483,647																						
CMPH	DINT [Array] *1	: -2,147,483,648 2,147,483,647																						
DONE	BOOL	"1" , 가 "0" "1" ,																						
STAT	USINT	가																						

1 : Array    4

4.2.5

(HSCB\_CNT)

가

		Datatype		
<div style="border: 1px solid black; padding: 5px; width: fit-content;">                     HSCB_CNT                      REQ DONE                      BASE STAT                      SLOT CNT                      CH LTCH_OLD                      SCNT_NEW                      TIME_A                      TIME_B                 </div>	REQ	BOOL	"0 1"	
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )	
	SLOT	USINT	: 0 7	
	CH	BOOL	"0" 0 , "1" 1	
	DONE	BOOL	"1" , 가 "0" "1"	
	STAT	USINT	가	
	CNT	DINT	: -2,147,483,648 2,147,483,647	
	LTCH_OLD	DINT	Latch	: -2,147,483,648 2,147,483,647
				: -2,147,483,648 2,147,483,647
	SCNT_NEW	DINT		: 0 -2,147,483,648 0 +2,147,483,647
				: -2,147,483,648 2,147,483,647
	TIME_A	UDINT	A ( ) : 1 25,000,000 ( )	
TIME_B	UDINT	B ( ) : 1 25,000,000 ( )		

4.2.6

(HSCB\_WR)

가/ , 가 , Carry/Borrow , 가  
/ , / 가

		Datatype	
<div style="border: 1px solid black; padding: 5px; width: fit-content;">                     HSCB_WR                      REQ DONE                      BASE STAT                      SLOT                      CH                      CNT_E                      PRE_E                      DOWN                      AUX_E                      CY_R                      PRE_I/E                      AUX_I/E                      PRE_R                      AUX_R                 </div>	REQ	BOOL	"0" 1
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )
	SLOT	USINT	: 0 7
	CH	BOOL	"0" 0 , "1" 1
	CNT_E	BOOL	가/
	PRE_E	BOOL	"0" "1" 가
	DOWN	BOOL	가/ "0" 가 가 "1" 가
	AUX_E	BOOL	가 가/ "0" 가 "1" 가 가
	CY_R	BOOL	가 Carry/Borrow가 , CY(Carry), BW(Borrow) "0" CY, BW "1" CY, BW Off(0)
	PRE_I/E	BOOL	"0" "1"
	AUX_I/E	BOOL	가 / "0" "1"
	PRE_R	BOOL	"0" On(1) "1" Off(0)
	AUX_R	BOOL	가 "0" On(1) "1" Off(0)
	DONE	BOOL	"1" , 가 "0" "1"
	STAT	USINT	가

4.2.7

(HSCB\_RD)

가/ , /  
 , Carry/Borrow 가

		Datatype	
<div style="border: 1px solid black; padding: 5px; width: fit-content;">                     HSCB_RD                      REQ DONE                      BASE STAT                      SLOT DOWN_F                      CH PRE_F                      AUX_F                      CY                      BW                      AUX_ING                 </div>	REQ	BOOL	"0" "1"
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )
	SLOT	USINT	: 0 7
	CH	BOOL	"0" 0 , "1" 1
	DONE	BOOL	"1" , 가 "0" "1"
	STAT	USINT	가
	DOWN_F	BOOL	가/ "0" 가 가 "1" 가
	PRE_F	BOOL	"0" 가 Off(0) "1" 가 On(1)
	AUX_F	BOOL	"0" 가 Off(0) "1" 가 On(1)
	CY	BOOL	가 Carry (Carry ) 2,147,483,647(LINEAR ) (RING ) "0" Carry가 "1" Carry가
	BW	BOOL	Borrow (Borrow ) -2,147,483,648(LINEAR ) (RING ) "0" Borrow가 "1" Borrow가
	AUX_ING	BOOL	가 "0" 가 "1" 가

4.2.8

(HSCB\_OUT)

Equal

		Datatype	
<div style="border: 1px solid black; padding: 2px;">                     HSCB_OUT                      - REQ DONE                      - BASE STAT                      - SLOT OUT0                      - CH OUT1                      - CMP_E OUT2                      - OUT_E OUT3                      - EQ0_R                      - EQ1_R                      - EQ2_R                      - EQ3_R                 </div>	REQ	BOOL	"0" "1"
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )
	SLOT	USINT	: 0 7
	CH	BOOL	"0" 0, "1" 1
	CMP_E	BOOL	"0" 가/ "1" 가
	OUT_E	BOOL	"0" OUT0/OUT1/OUT2/OUT3 "1" OUT0/OUT1/OUT2/OUT3 가
	EQ0_R	BOOL	Equal (=) (OUT0) "1" (OUT0) Equal
	EQ1_R	BOOL	Equal (=) (OUT1) "1" (OUT1) Equal
	EQ2_R	BOOL	Equal (=) (OUT2) "1" (OUT2) Equal
	EQ3_R	BOOL	Equal (=) (OUT3) "1" (OUT3) Equal
	DONE	BOOL	"1" , 가 "0" "1"
	STAT	USINT	가
	OUT0	BOOL	OUT0 "0" Off "1" On
	OUT1	BOOL	OUT1 "0" Off "1" On
	OUT2	BOOL	OUT2 "0" Off "1" On
OUT3	BOOL	OUT3 "0" Off "1" On	

4.3

4.3.1

(HSCBRPRE)

		Datatype	
<div style="border: 1px solid black; padding: 2px; width: fit-content;">                     HSCBRPRE                      - REQ    DONE                      - NET_    ERR                      - ST_N    STAT                      - O                      - BASE                      - SLOT                      - CH                      - PSET                 </div>	REQ	BOOL	(Preset) "0 1"
	NET_NO	USINT	: 0 7
	ST_NO	USINT	I/O : 0 63
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )
	SLOT	USINT	: 0 7
	CH	BOOL	"0" 0 , "1" 1
	PSET	DINT	: -2,147,483,648 2,147,483,647
	DONE	BOOL	(Preset) "1" , 가 "0"
	ERR	BOOL	가 "1" , 가 "1" , "0"
	STAT	USINT	(Preset) 가

4.3.2

(HSCBRMOD)

		Datatype																	
<div style="border: 1px solid black; padding: 2px;">                     HSCBRMOD                      REQ DONE                      NET_NO ERR                      ST_NO STAT                      BASE                      SLOT                      CH                      MODE                      SEL                      RING_L                      RING_H                 </div>	REQ	BOOL	"0 1"																
	NET_NO	USINT	: 0 7																
	ST_NO	USINT	I/O : 0 63																
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )																
	SLOT	USINT	: 0 7																
	CH	BOOL	"0" 0 , "1" 1																
	MODE	USINT	: 0 7																
			<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>0</td><td>2 1</td></tr> <tr><td>1</td><td>2 2</td></tr> <tr><td>2</td><td>2 4</td></tr> <tr><td>3</td><td>CW/CCW</td></tr> <tr><td>4</td><td>1 1 1 ( 가 )</td></tr> <tr><td>5</td><td>1 1 2 ( 가 )</td></tr> <tr><td>6</td><td>1 2 1 (B 가 )</td></tr> <tr><td>7</td><td>1 2 2 (B 가 )</td></tr> </table>	0	2 1	1	2 2	2	2 4	3	CW/CCW	4	1 1 1 ( 가 )	5	1 1 2 ( 가 )	6	1 2 1 (B 가 )	7	1 2 2 (B 가 )
	0	2 1																	
	1	2 2																	
	2	2 4																	
	3	CW/CCW																	
	4	1 1 1 ( 가 )																	
	5	1 1 2 ( 가 )																	
6	1 2 1 (B 가 )																		
7	1 2 2 (B 가 )																		
SEL	BOOL	0 : Linear 1 : Ring																	
RING_L	DINT	Ring : -2,147,483,648 2,147,483,647																	
RING_H	DINT	Ring : -2,147,483,648 2,147,483,647																	
DONE	BOOL	"1" , 가 "0" , "1"																	
ERR	BOOL	가 "1" , 가 "0"																	
STAT	USINT	가																	

4.3.3 가 (HSCBRAUX) 가

가

가

		Datatype													
<div style="border: 1px solid black; padding: 2px;">                     SCBRAUX                      REQ DONE                      NET_N ERR                      O                      ST_N STAT                      O                      BASE                      SLOT                      CH                      AUX                      SET                      TIME                 </div>	REQ	BOOL	가 "0 1"												
	NET_NO	USINT	: 0 7												
	ST_NO	USINT	1/0 : 0 63												
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )												
	SLOT	USINT	: 0 7												
	CH	BOOL	"0" 0 , "1" 1												
	AUX	USINT	가 : 0 5 <table border="1" style="margin-left: 20px;"> <tr><td>0</td><td>가</td></tr> <tr><td>1</td><td>Clear</td></tr> <tr><td>2</td><td>Latch</td></tr> <tr><td>3</td><td></td></tr> <tr><td>4</td><td></td></tr> <tr><td>5</td><td></td></tr> </table>	0	가	1	Clear	2	Latch	3		4		5	
	0	가													
	1	Clear													
	2	Latch													
3															
4															
5															
SET_TIME	UINT	: 1 65,535 (ms)													
		: 1 65,535 (ms)													
DONE	BOOL	가 "1" , 가 "0" , "1"													
ERR	BOOL	가 "1" 가 "1" , "0"													
STAT	USINT	가 가													

4.3.4

(HSCBRCMP)

/

		Datatype																						
HSCBRCMP REQ DONE NET_NO ERR ST_NO STAT O BASE SLOT CH CMPS CMPL CMPH	REQ	BOOL	"0 1"																					
	NET_NO	USINT	: 0 7																					
	ST_NO	USINT	1/0 : 0 63																					
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )																					
	SLOT	USINT	: 0 7																					
	CH	BOOL	"0" 0 , "1" 1																					
	CMPS	USINT [Array] *1	: 0 6 <table border="1" style="margin-left: 20px;"> <tr><td>0</td><td>&lt;</td><td>:</td></tr> <tr><td>1</td><td></td><td>:</td></tr> <tr><td>2</td><td>=</td><td>:</td></tr> <tr><td>3</td><td></td><td>:</td></tr> <tr><td>4</td><td>&gt;</td><td>:</td></tr> <tr><td>5</td><td></td><td>:</td></tr> <tr><td>6</td><td>.</td><td>:</td></tr> </table>	0	<	:	1		:	2	=	:	3		:	4	>	:	5		:	6	.	:
	0	<	:																					
	1		:																					
	2	=	:																					
3		:																						
4	>	:																						
5		:																						
6	.	:																						
CMPL	DINT [Array] *1	: -2,147,483,648 2,147,483,647																						
CMPH	DINT [Array] *1	: -2,147,483,648 2,147,483,647																						
DONE	BOOL	"1" , 가 "0" "1" ,																						
ERR	BOOL	가 "1" 가 "1" , "0"																						
STAT	USINT	가																						

1 : Array 4 .

4.3.5

(HSCBRCNT)

가

			Datatype	
<div style="border: 1px solid black; padding: 2px;">                     HSCBRCNT                      REQ DONE                      NET_ ERR                      NO_ ST_N                      ST_N STAT                      O_ STAT                      BASE CNT                      CNT                      SLOT LTCH                      LTCH_OLD                      CH SCNT                      SCNT_NEW                      TIME_A                      TIME_B                 </div>		REQ	BOOL	"0 1"
		NET_NO	USINT	: 0 7
		ST_NO	USINT	1/0 : 0 63
		BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )
		SLOT	USINT	: 0 7
		CH	BOOL	"0" 0 , "1" 1
		DONE	BOOL	"1" , 가 "0" , "1"
		ERR	BOOL	가 "1" 가 "1" , "0"
		STAT	USINT	가
		CNT	DINT	: -2,147,483,648 2,147,483,647
		LTCH_OLD	DINT	Latch : -2,147,483,648 2,147,483,647
				: -2,147,483,648 2,147,483,647
		SCNT_NEW	DINT	: 0 -2,147,483,648 0 +2,147,483,647
				: -2,147,483,648 2,147,483,647
	TIME_A	UDINT	A ( ) : 1 25,000,000 ( )	
	TIME_B	UDINT	B ( ) : 1 25,000,000 ( )	

4.3.6

(HSCBRWR)

가/ , 가 , Carry/Borrow , 가  
/ , / 가

		Datatype	
<div style="border: 1px solid black; padding: 5px;">                     HSCBRWR                      REQ DONE                      NET_NO ERR                      ST_NO STAT                      BASE                      SLOT                      CH                      CNT_E                      PRE_E                      DOWN                      AUX_E                      CY_R                      PRE_I/E                      AUX_I/E                      PRE_R                      AUX_R                 </div>	REQ	BOOL	"0 1"
	NET_NO	USINT	: 0 7
	ST_NO	USINT	1/0 : 0 63
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )
	SLOT	USINT	: 0 7
	CH	BOOL	"0" 0 , "1" 1
	CNT_E	BOOL	가/ "0" "1" 가
	PRE_E	BOOL	가/ "0" "1" 가
	DOWN	BOOL	가/ "0" 가 가 "1" 가
	AUX_E	BOOL	가 가/ "0" 가 "1" 가 가
	CY_R	BOOL	가 Carry/Borrow가 , CY(Carry), BW(Borrow) "0" CY, BW "1" CY, BW Off(0)
	PRE_I/E	BOOL	"0" "1"
	AUX_I/E	BOOL	가 / "0" "1"
	PRE_R	BOOL	"0" On(1) "1" Off(0)
	AUX_R	BOOL	가 "0" On(1) "1" Off(0)
	DONE	BOOL	"1" , 가 "0"
	ERR	BOOL	가 "1" 가 "1" , "0"
	STAT	USINT	가

4.3.7

(HSCBRRD)

가/ , /  
 , Carry/Borrow 가

		Datatype	
HSCBRRD + REQ DONE + NET_ ERR NO + ST_N STAT O DOWN BASE F + SLOT PRE F CH AUX_ F CY BW AUX_ ING	REQ	BOOL	"0" 1
	NET_NO	USINT	: 0 7
	ST_NO	USINT	1/0 : 0 63
	BASE	USINT	: GM4 (0 3), GM6 : 0~1(12 )
	SLOT	USINT	: 0 7
	CH	BOOL	"0" 0 , "1" 1
	DONE	BOOL	"1" , 가 "0" "1" ,
	ERR	BOOL	가 "1" 가 "1" , "0"
	STAT	USINT	가
	DOWN_F	BOOL	가/ "0" 가 가 "1" 가
	PRE_F	BOOL	"0" 가 Off(0) "1" 가 On(1)
	AUX_F	BOOL	"0" 가 Off(0) "1" 가 On(1)
	CY	BOOL	가 Carry (Carry ) 2,147,483,647(LINEAR ) (RING) "0" Carry가 "1" Carry가
	BW	BOOL	Borrow (Borrow ) -2,147,483,648(LINEAR ) (RING) "0" Borrow가 "1" Borrow가
AUX_ING	BOOL	가 "0" 가 "1" 가	

4.3.8

(HSCBROUT)

Equal

		Datatype	
<div style="border: 1px solid black; padding: 2px;">                     HSCBROUT                      REQ DONE                      NET_NO ERR                      ST_NO STAT                      BASE OUT0                      SLOT OUT1                      CH OUT2                      CMP_E OUT3                      OUT_E                      EQ0_R                      EQ1_R                      EQ2_R                      EQ3_R                 </div>	REQ	BOOL	"0" 1
	NET_NO	USINT	: 0 7
	ST_NO	USINT	1/0 : 0 63
	BASE	USINT	: GM4 (0 3), GM6 : 0~1 (12 )
	SLOT	USINT	: 0 7
	CH	BOOL	"0" 0, "1" 1
	CMP_E	BOOL	"0" 가/ "1" 가
	OUT_E	BOOL	"0" OUT0/OUT1/OUT2/OUT3 "1" OUT0/OUT1/OUT2/OUT3 가
	EQ0R	BOOL	(OUT0) Equal CMPS[0] Equal(=) "0" (OUT0) Equal Equal "1" (OUT0) Equal
	EQ1R	BOOL	(OUT1) Equal CMPS[1] Equal(=) "0" (OUT1) Equal Equal "1" (OUT1) Equal
	EQ2R	BOOL	(OUT2) Equal CMPS[2] Equal(=) "0" (OUT2) Equal Equal "1" (OUT2) Equal
	EQ3R	BOOL	(OUT3) Equal CMPS[3] Equal(=) "0" (OUT3) Equal Equal "1" (OUT3) Equal
	DONE	BOOL	"1" 가 "0" "1"
	ERR	BOOL	가 "1" 가 "1" "0"
	STAT	USINT	가
	OUT0	BOOL	OUT0 "0" Off "1" On
	OUT1	BOOL	OUT1 "0" Off "1" On
OUT2	BOOL	OUT2 "0" Off "1" On	

		OUT3	BOOL	OUT3 " 0 "      Off " 1 "      On
--	--	------	------	---

4.4

STAT

STAT			
1		가	(4.2 )
2		H/W	A/S
3		가	
4			
5			
6			
7		H/W	A/S
8			A/S
9			
128		H/W	
129		가	(4.3 )
131		가	
133			A/D
135		H/W	A/S
136			A/S
137			

5.1

1

G4F-H01A

GM4- PA2A	GM4- CPUA CPU	G4I- D22A 0	G4F- HO1A 1	G4Q- TR2A 2	G4Q- TR2A 3
--------------	---------------------	-------------------	-------------------	-------------------	-------------------

5.1.1

RPM

2 1

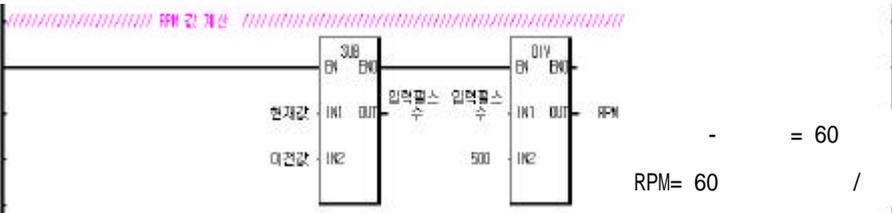
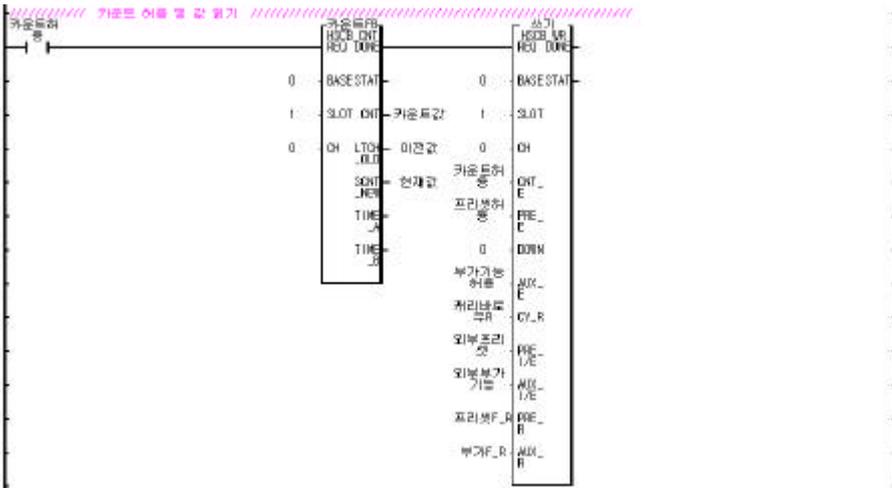
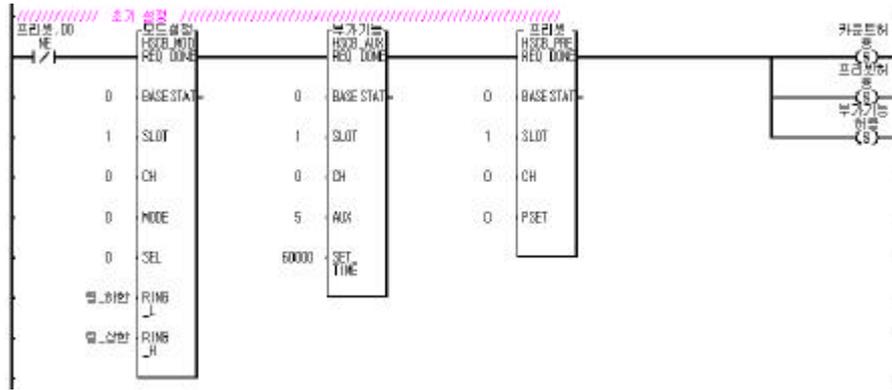
RPM

: PLC가

가

/

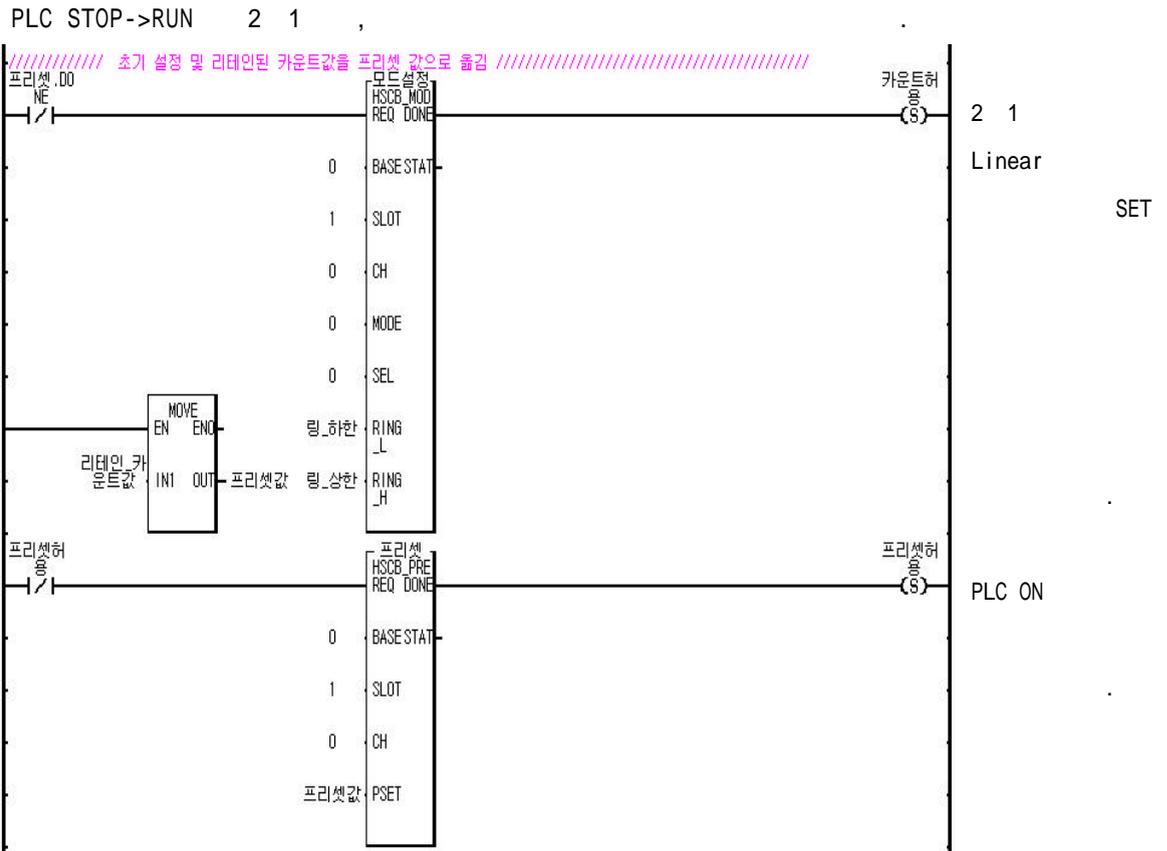
가

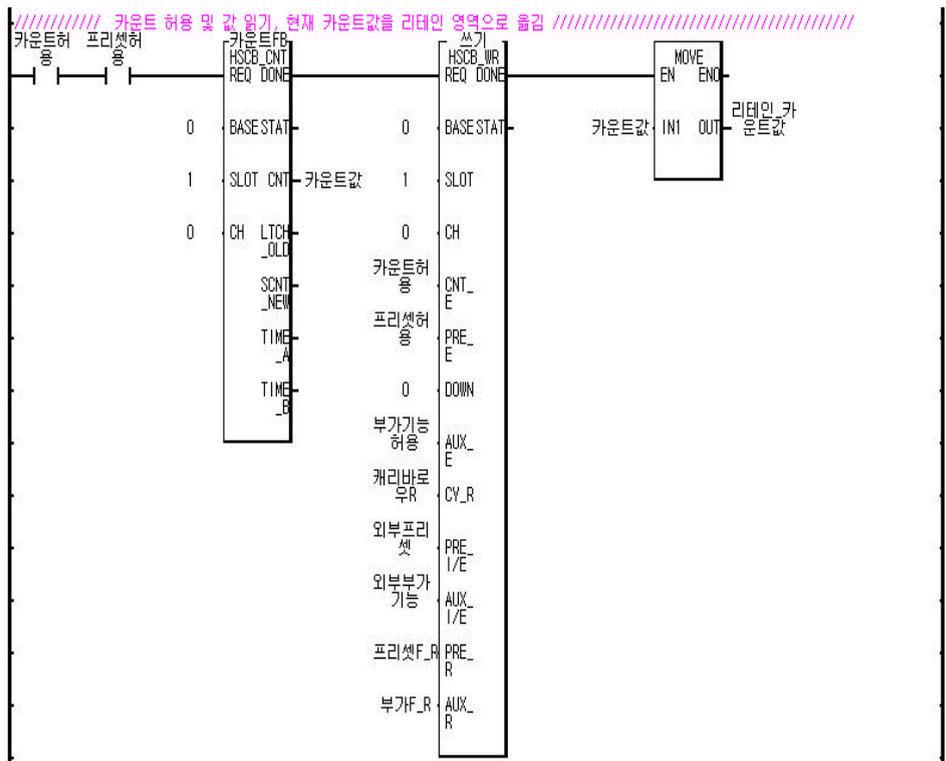


PLC	OFF	0	OFF
	0	PLC가 STOP	RUN 0

5.1.2

PLC가 , PLC OFF->ON  
 OFF  
 : PLC가 ,  
 ,PLC



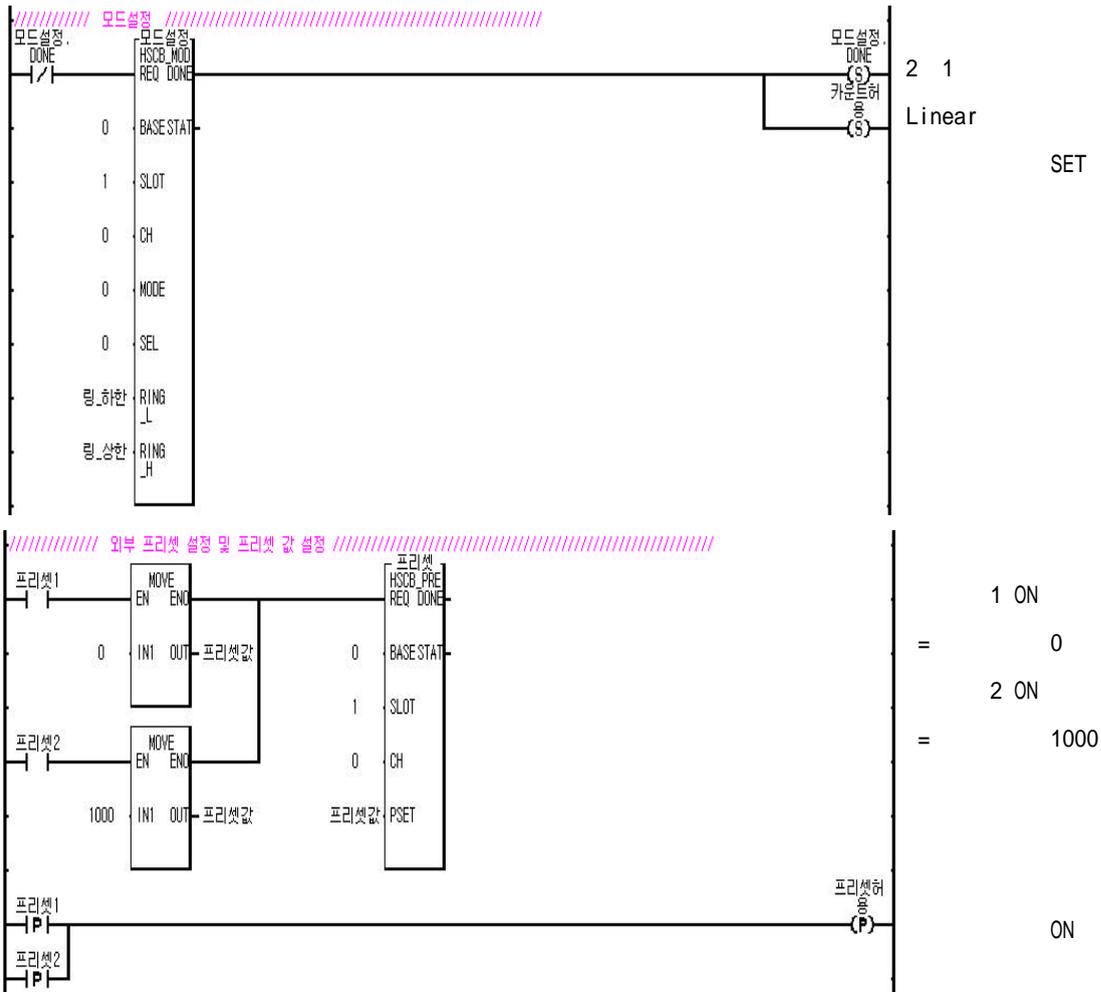


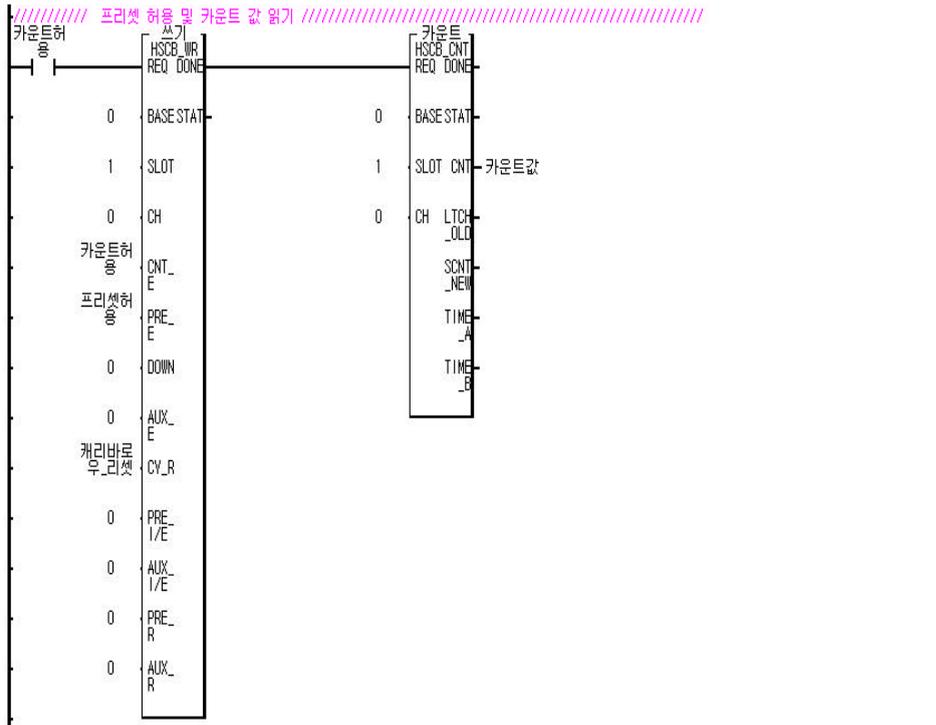
PLC가 STOP->RUN		,PLC	
OFF	0	.PLC	OFF

5.1.3

가

: 1 0 2 1000

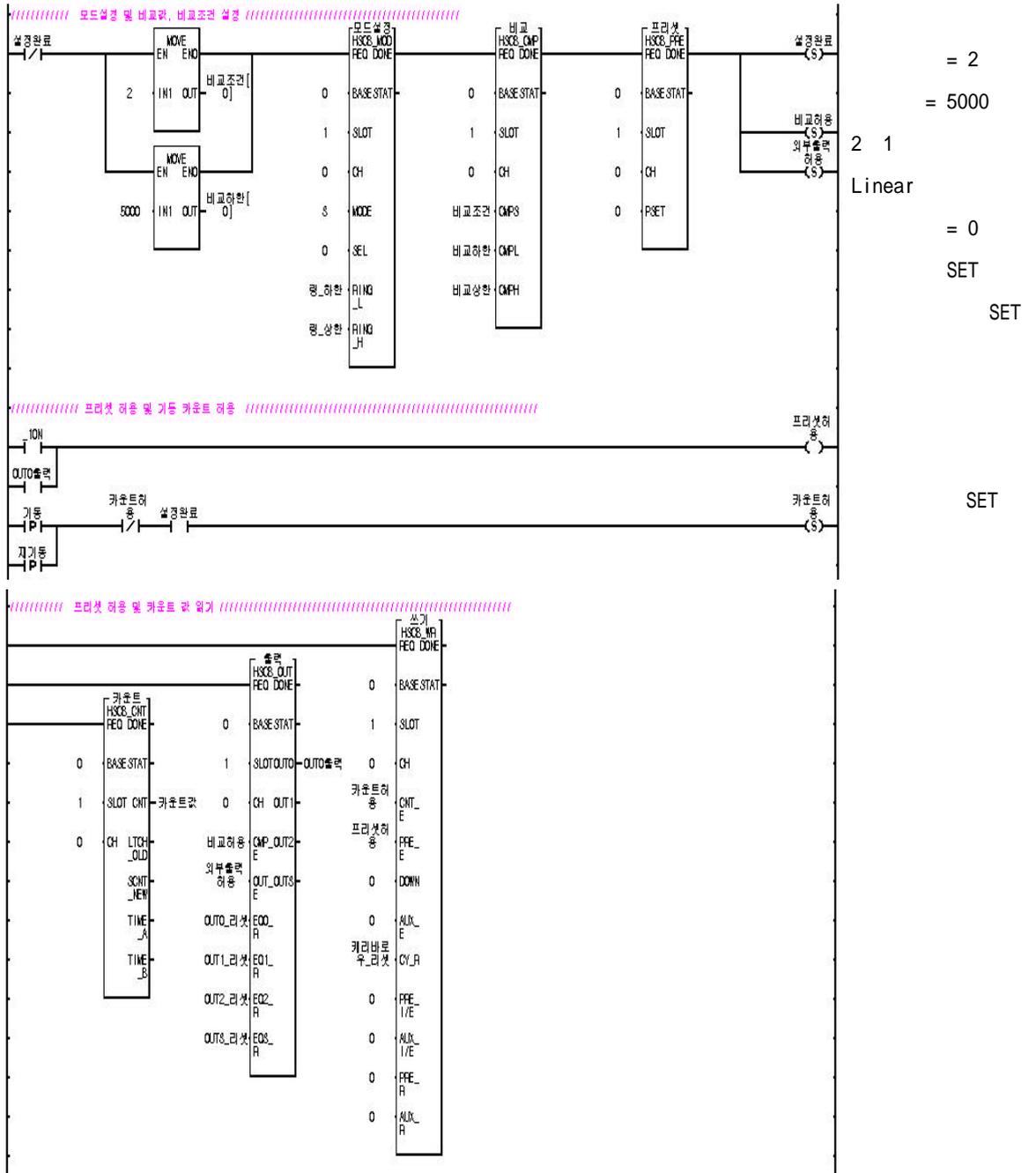




PLC	OFF	,	,	OFF
	(0)	.		
			HSCB_WR	PRE_I/E 1

5.1.4

0 OUT0  
 : 가 ON , 가 5000 가  
 , 5000 OUT0가 ON  
 가 ON 5000





4 .

" = "

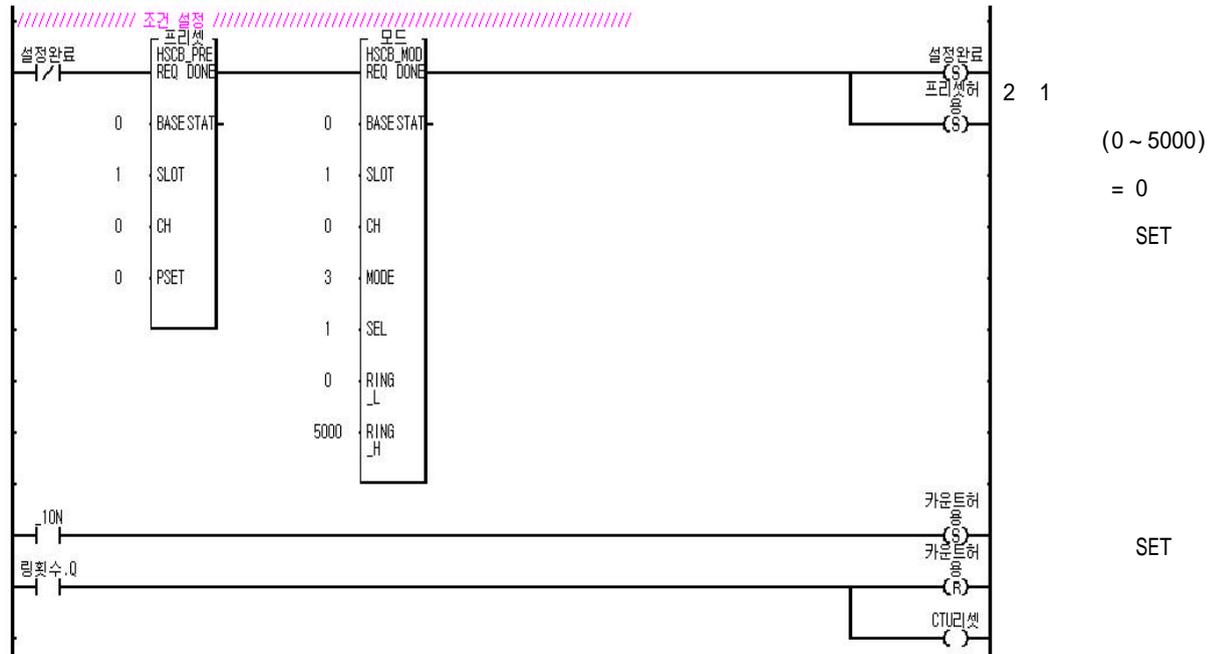
( OUTO\_ ) ON OFF .

ON ,

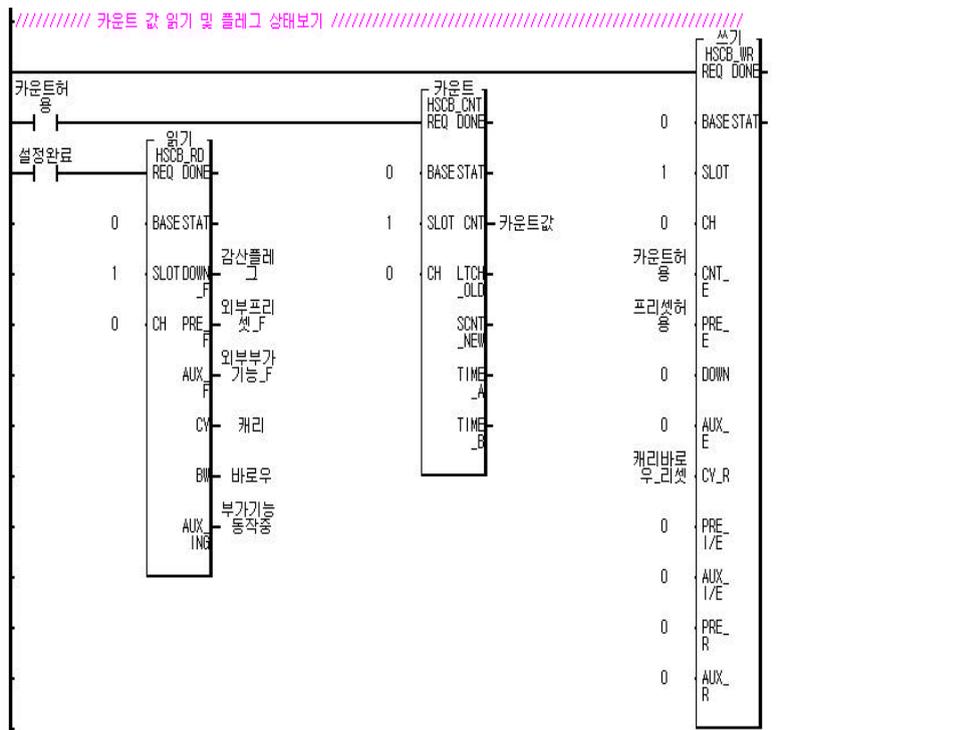
OFF .

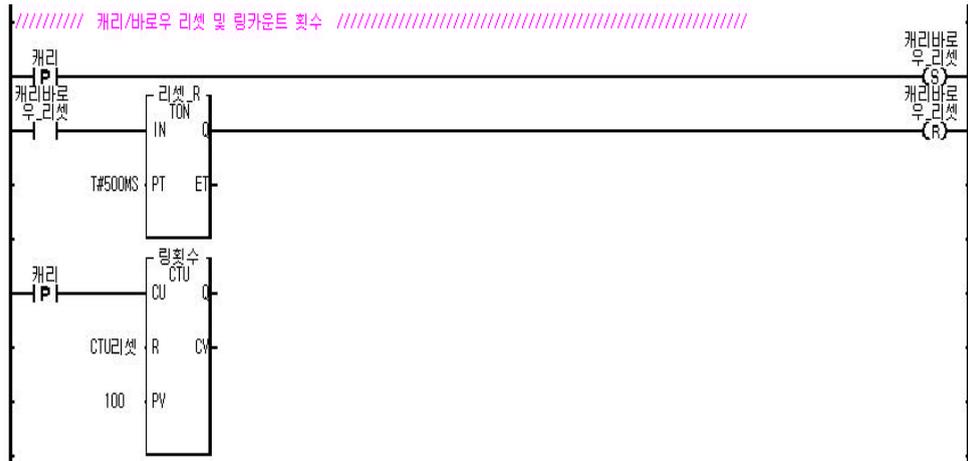
5.1.5 /

: , 100 (5000)  
 가 , 100

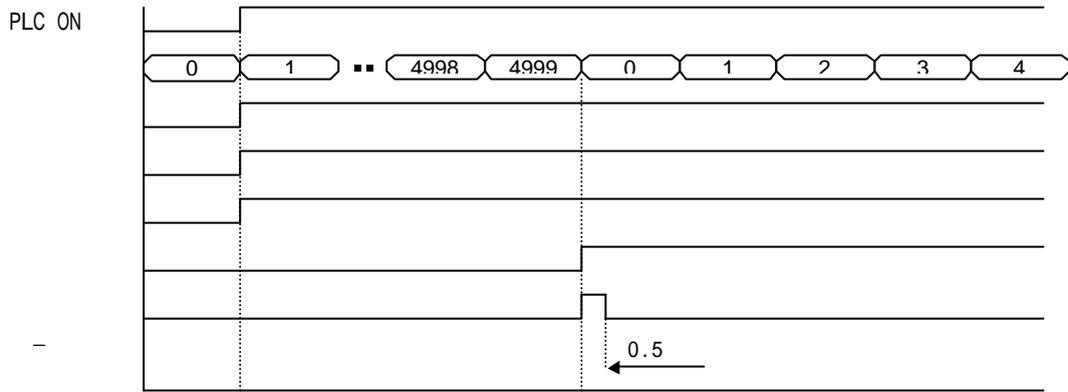


2.





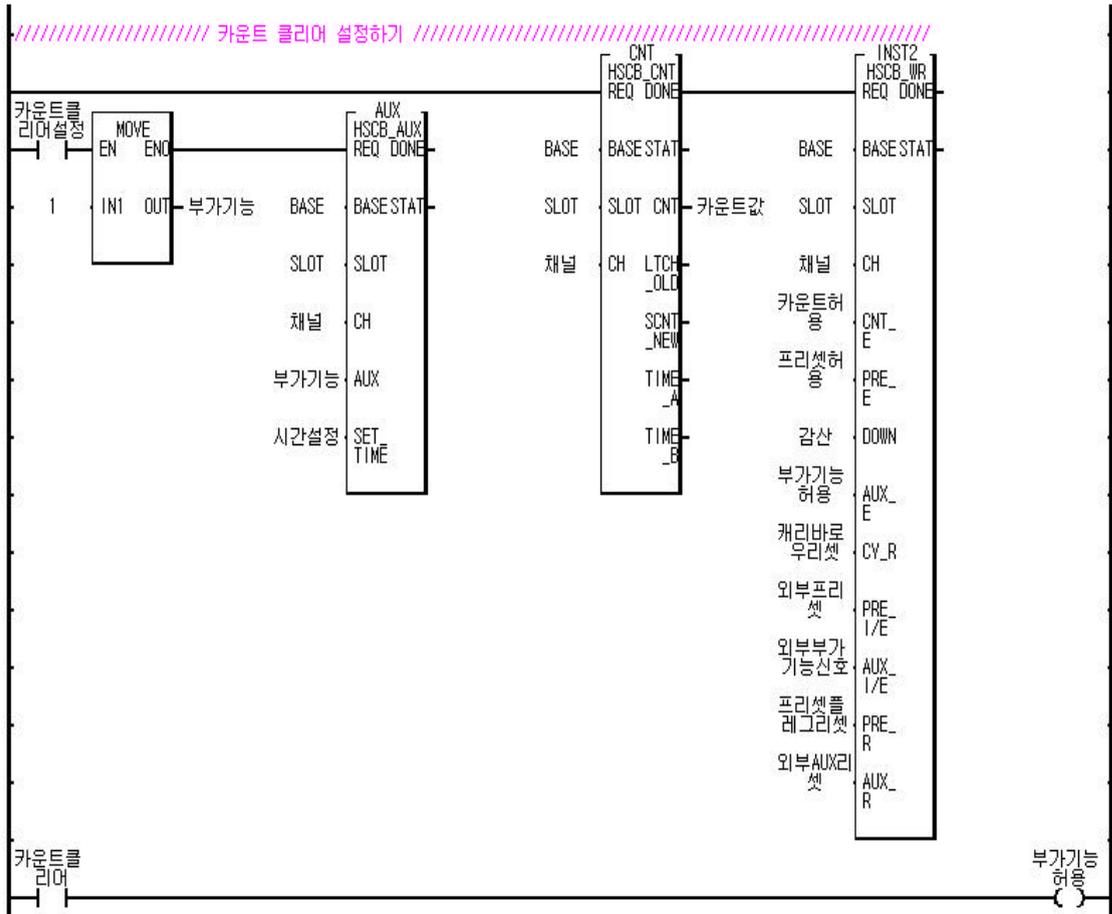
0.5



5.1.6 가  
1)

: HSCB\_AUX, HSCB\_WR  
가 (HSCB\_WR AUX\_E) On

: HSCB\_AUX AUX [1] -> 가  
On.



(Edge) . 가 가 On  
, On

2)

: HSCB\_AUX, HSCB\_WR, HSCB\_CNT

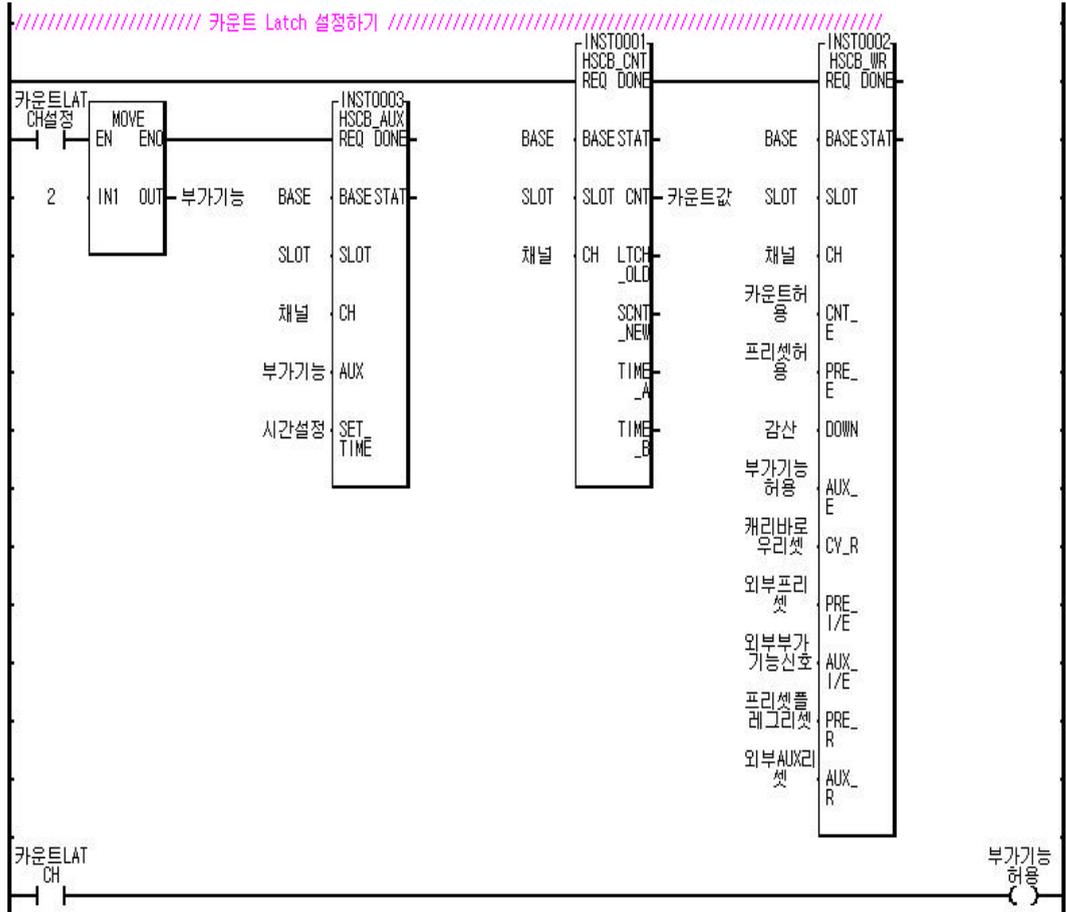
가 (HSCB\_WR AUX\_E) On HSCB\_CNT

LTCH\_OLD

: HSCB\_AUX AUX [2] -> 가

On.

가 가 On 가



3)

: HSCB\_AUX, HSCB\_WR, HSCB\_CNT

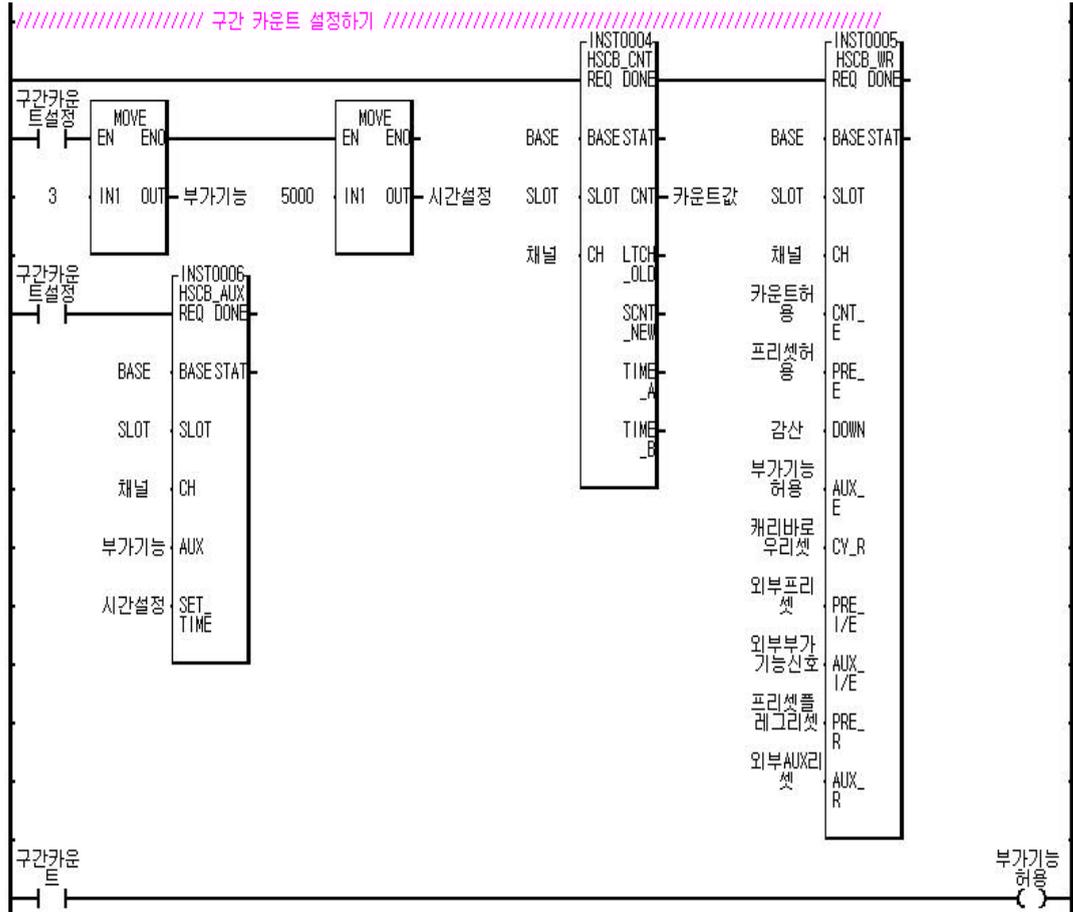
가 (HSCB\_WR AUX\_E) On

HSCB\_CNT SCNT\_NEW

: HSCB\_AUX AUX [3] ->SET\_TIME

-> 가 On.

가 가 On 가



4)

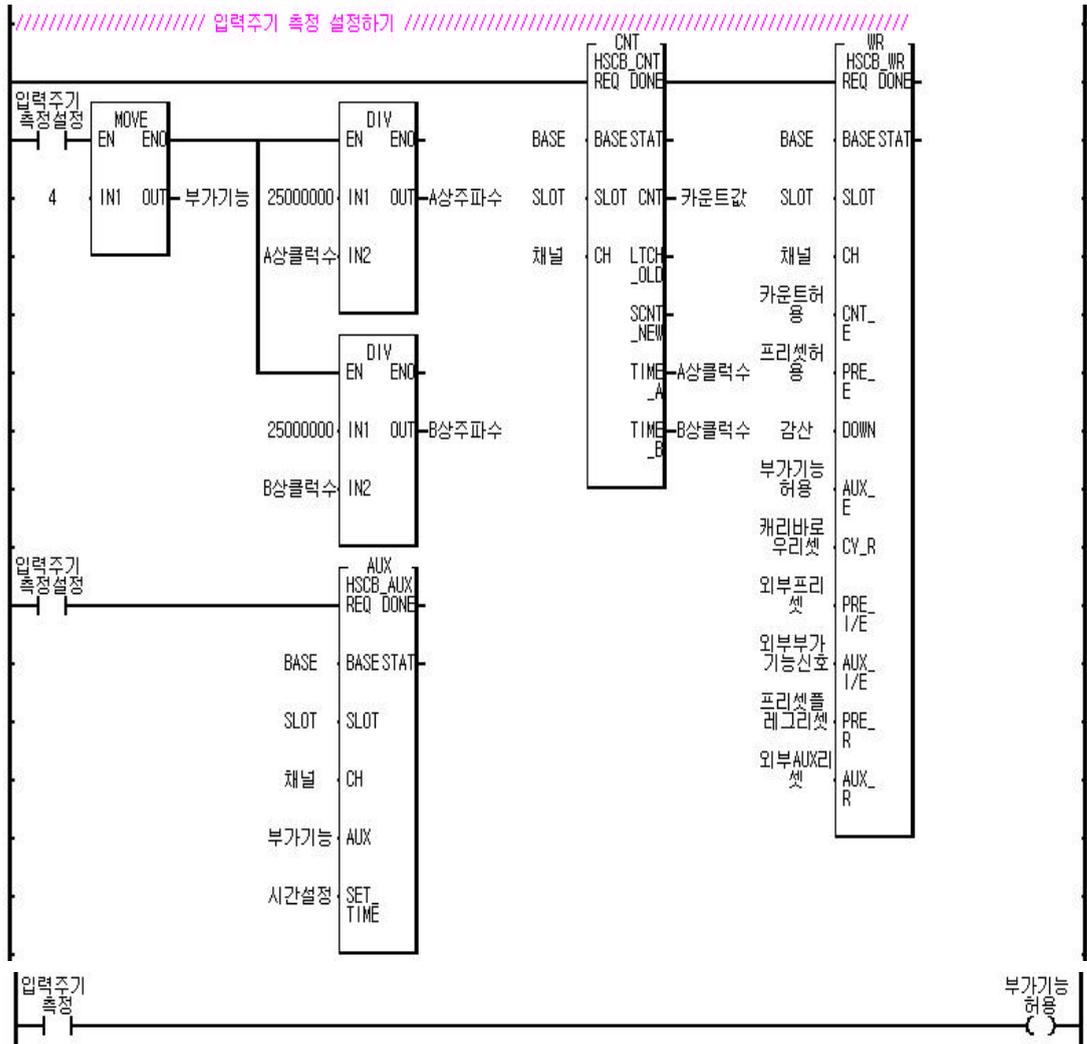
: HSCB\_AUX, HSCBWR, HSCB\_CNT

가 (HSCB\_WR AUX\_E)가 On A /B

HSCB\_CNT TIME\_A, TIME\_B .

: HSCB\_AUX AUX [4] -> 가

On.



5)

: HSCB\_AUX, HSCB\_WR, HSCB\_CNT

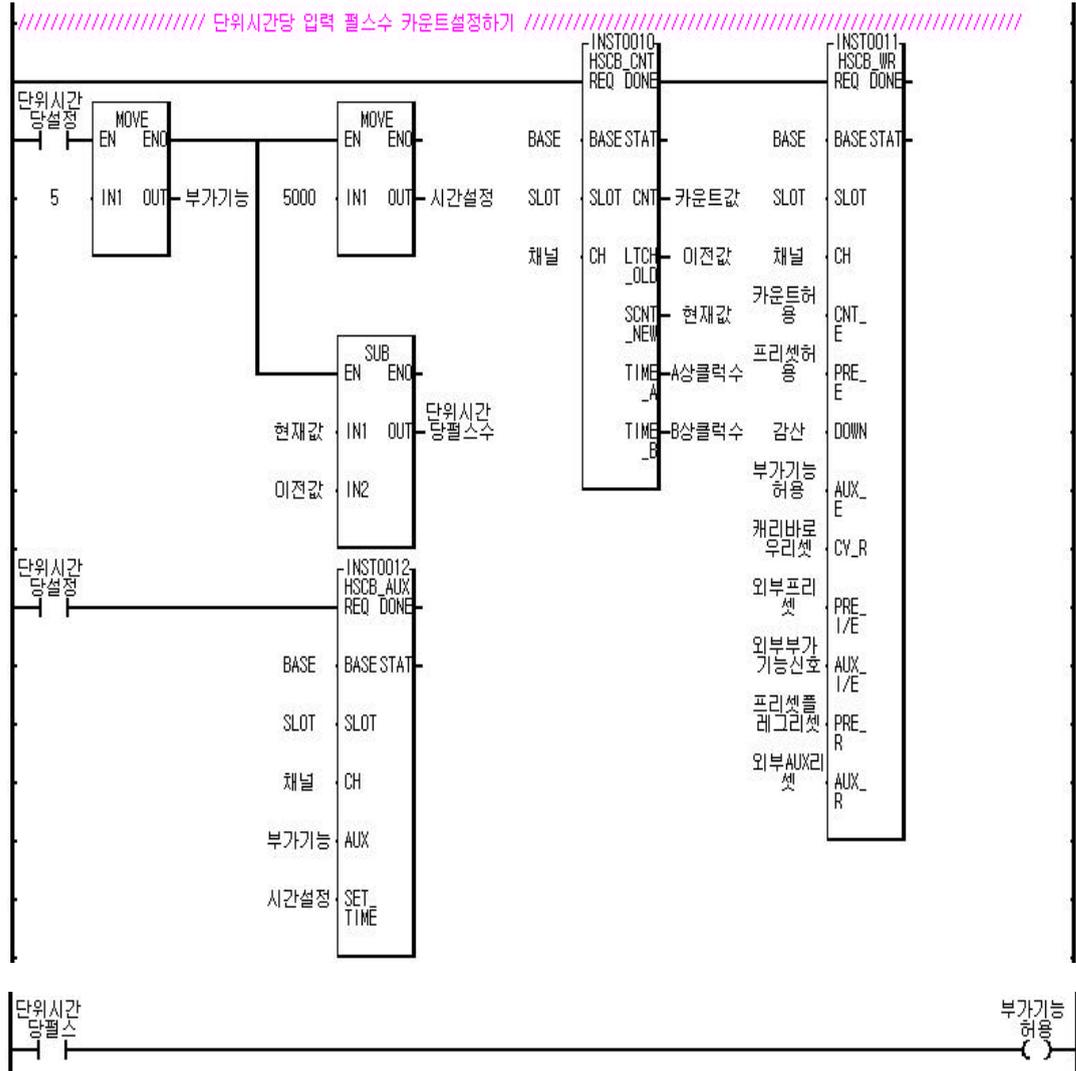
가 (HSCB\_WR AUX\_E) On Latch

HSCB\_CNT SCNT\_NEW LTCH\_OLD

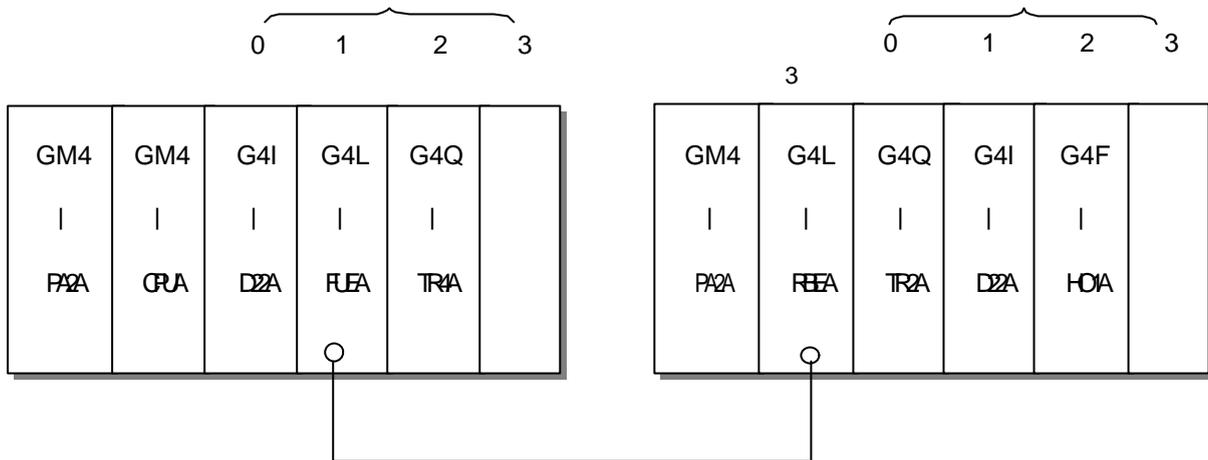
: HSCB\_AUX AUX [3] ->SET\_TIME

-> 가 On.

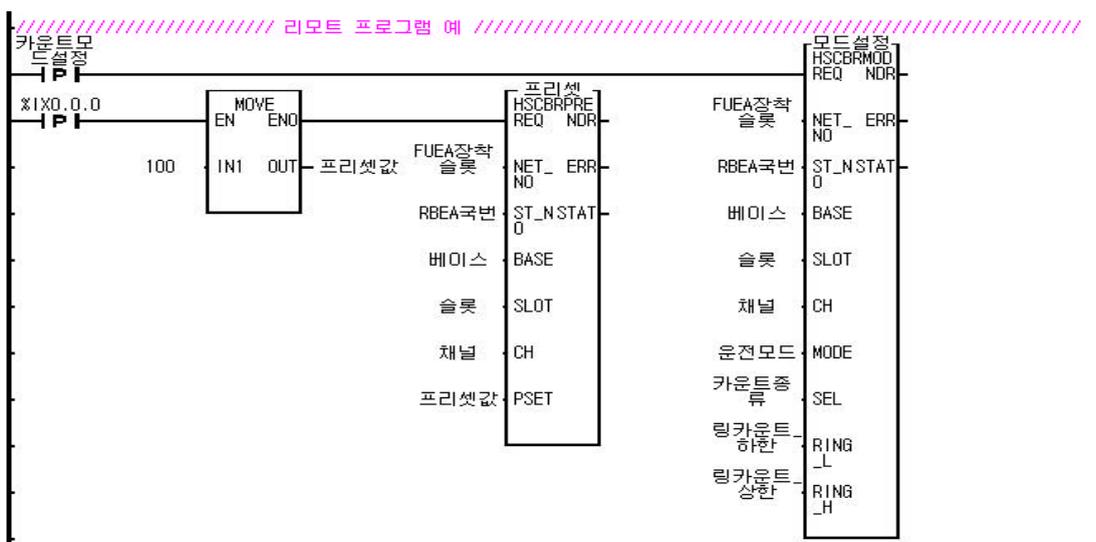
가 가 On

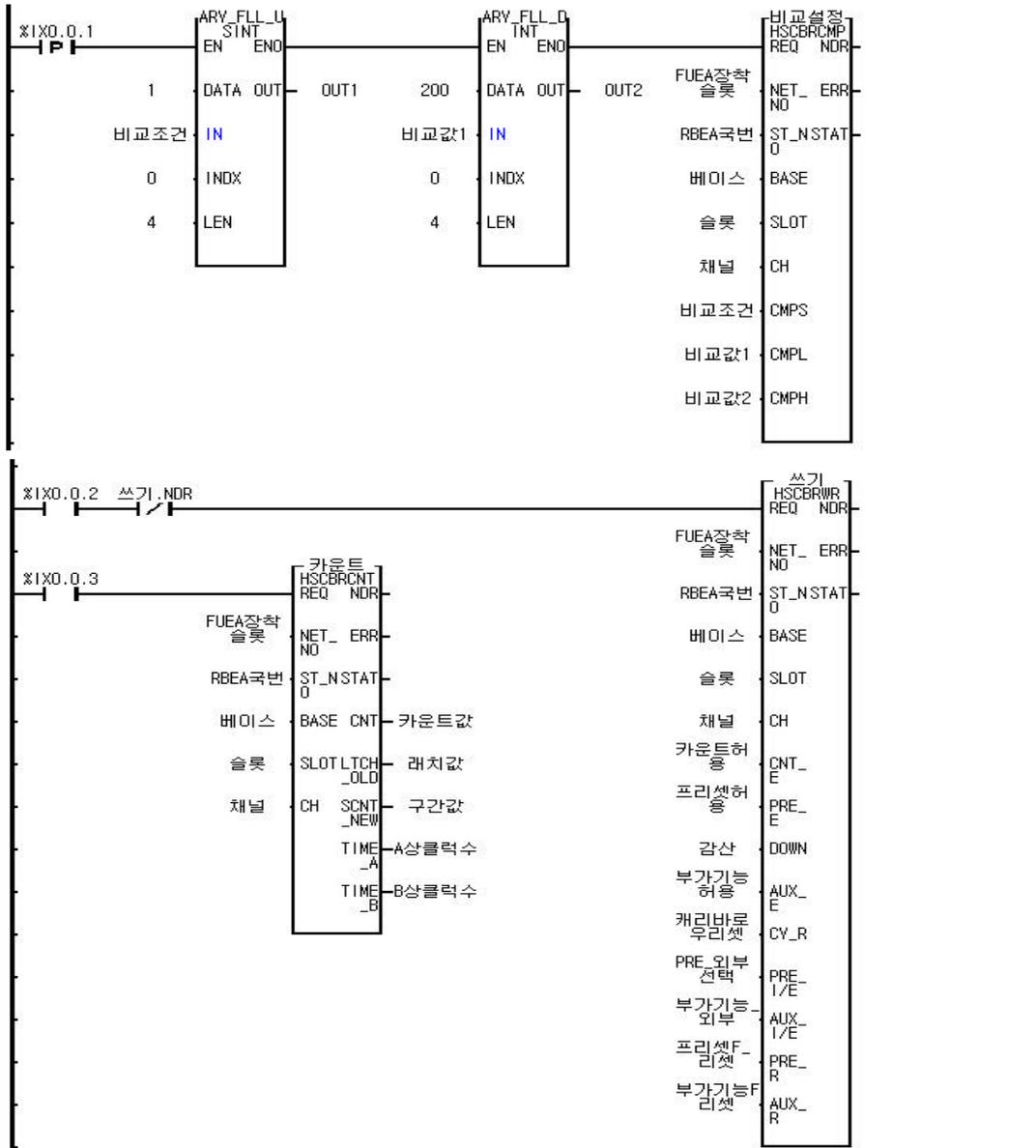


5.2 /



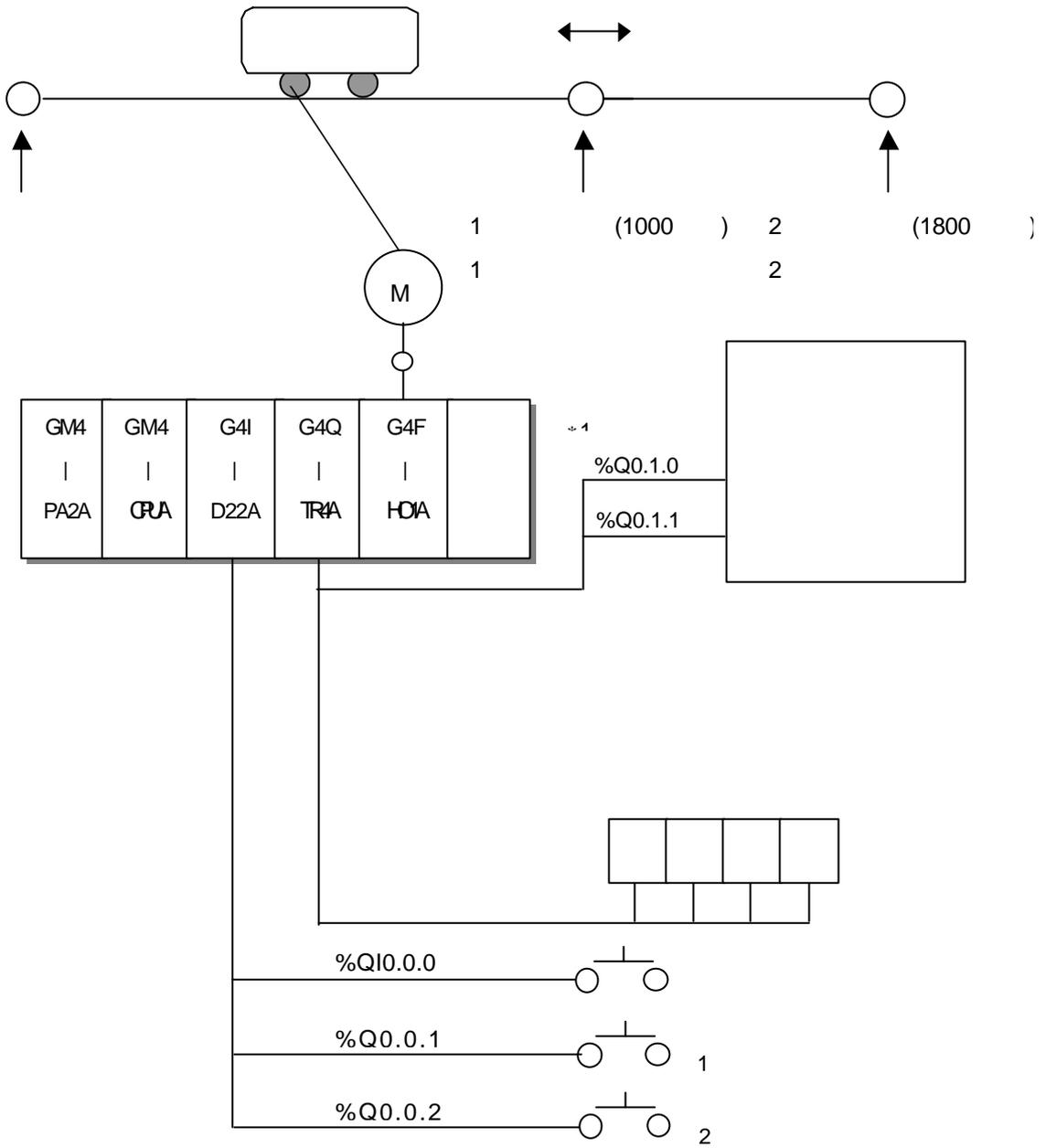
NET\_NO : G4L-FUEA가 = 1  
 ST\_NO : G4L-RBEA = 3  
 BASE : G4F-H01A가 = 0  
 SLOT : G4F-H01A가 = 2





5.3

5.3.1



%Q0.1.16 ~%Q0.1.31

- 가  
 1 .  
 - 1 가 On 2 . 2  
 가 On .

/

%I0.0.0 :

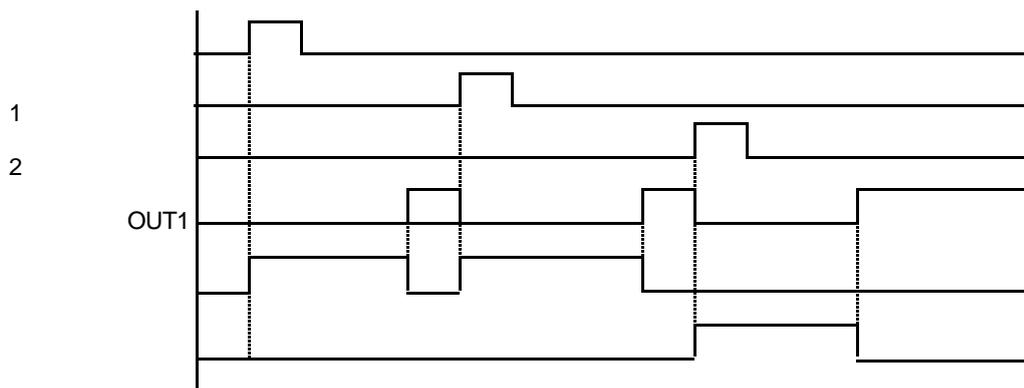
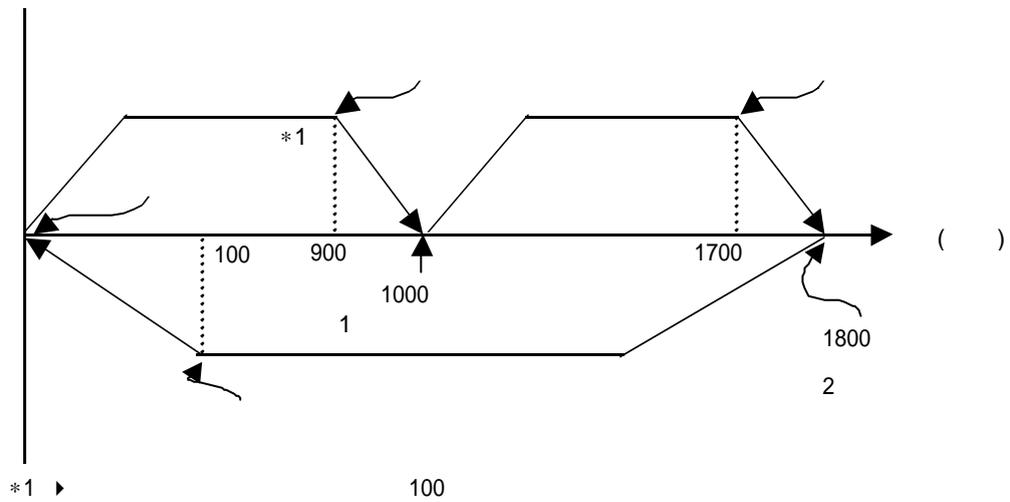
%I0.0.1 : 1

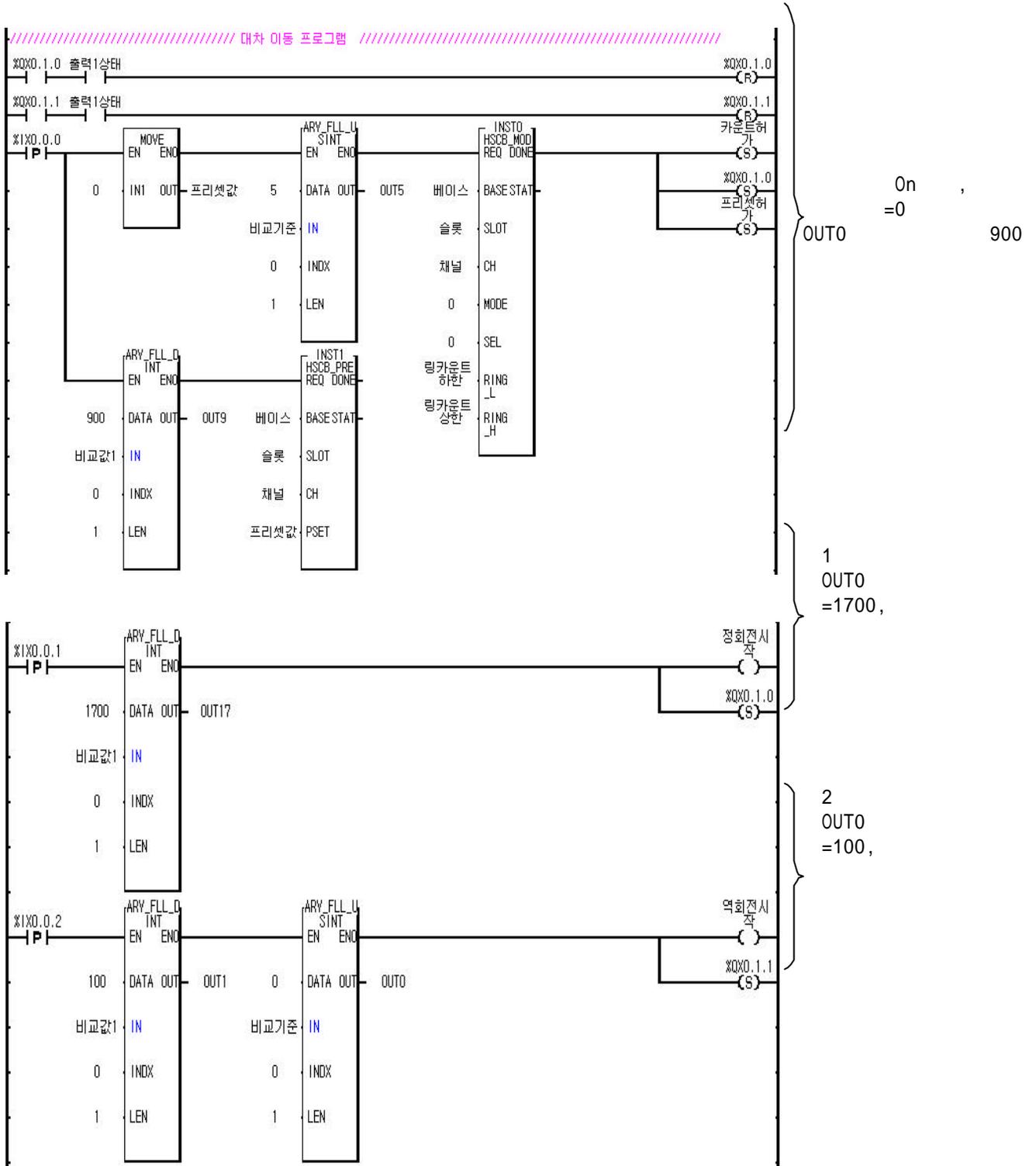
%I0.0.2 : 2

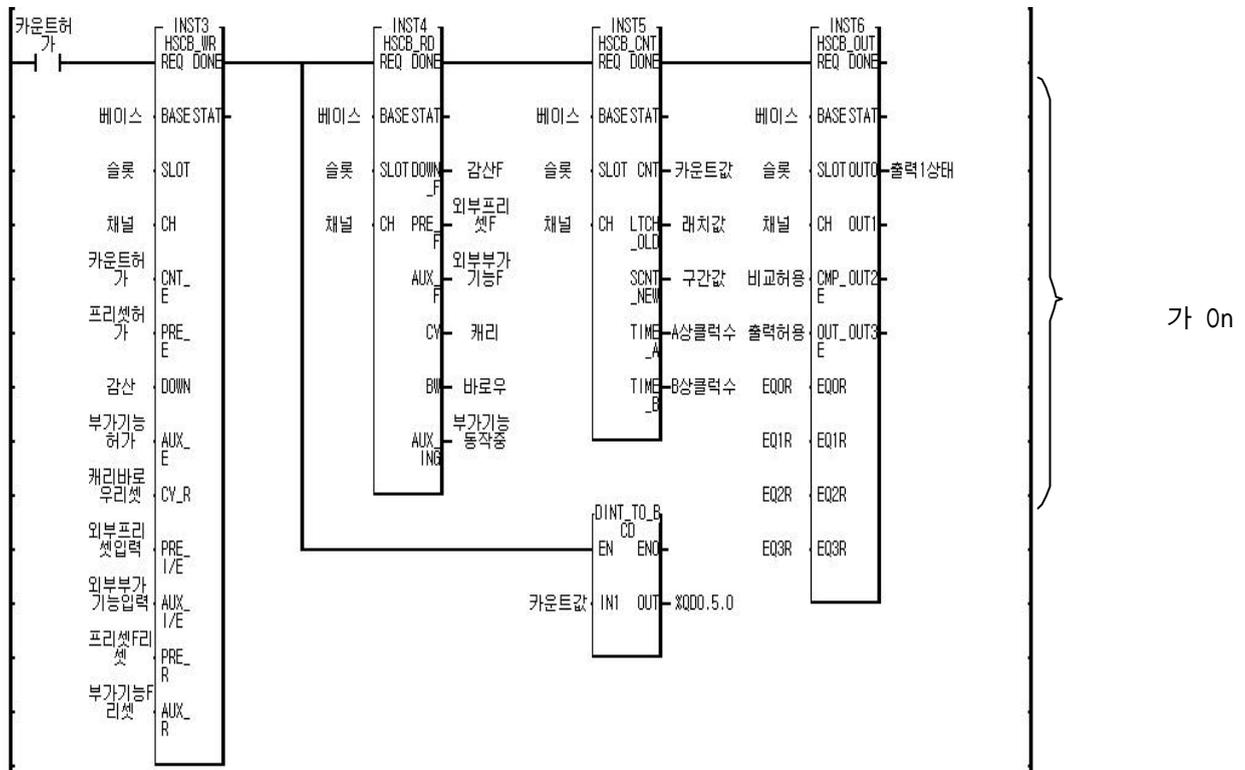
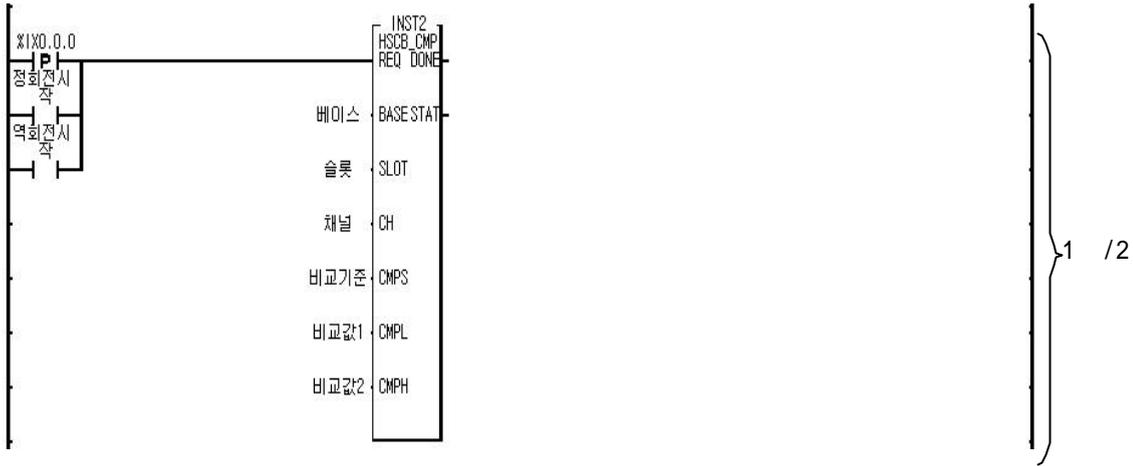
%Q0.1.0 : (On : , Off : )

%Q0.1.1 : (On : , Off : )

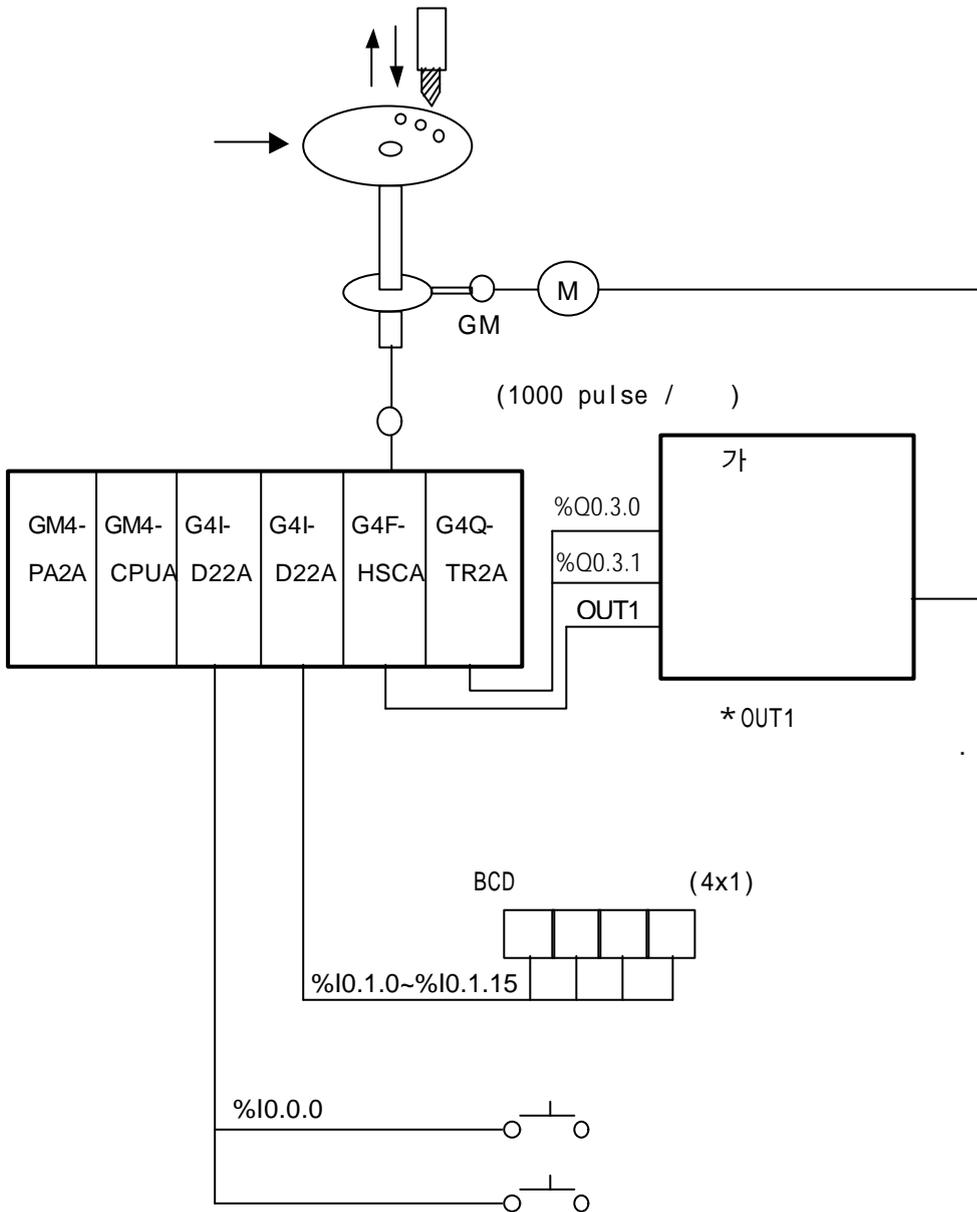
%IQ0.1.16 ~ %Q0.1.31 : (BCD)





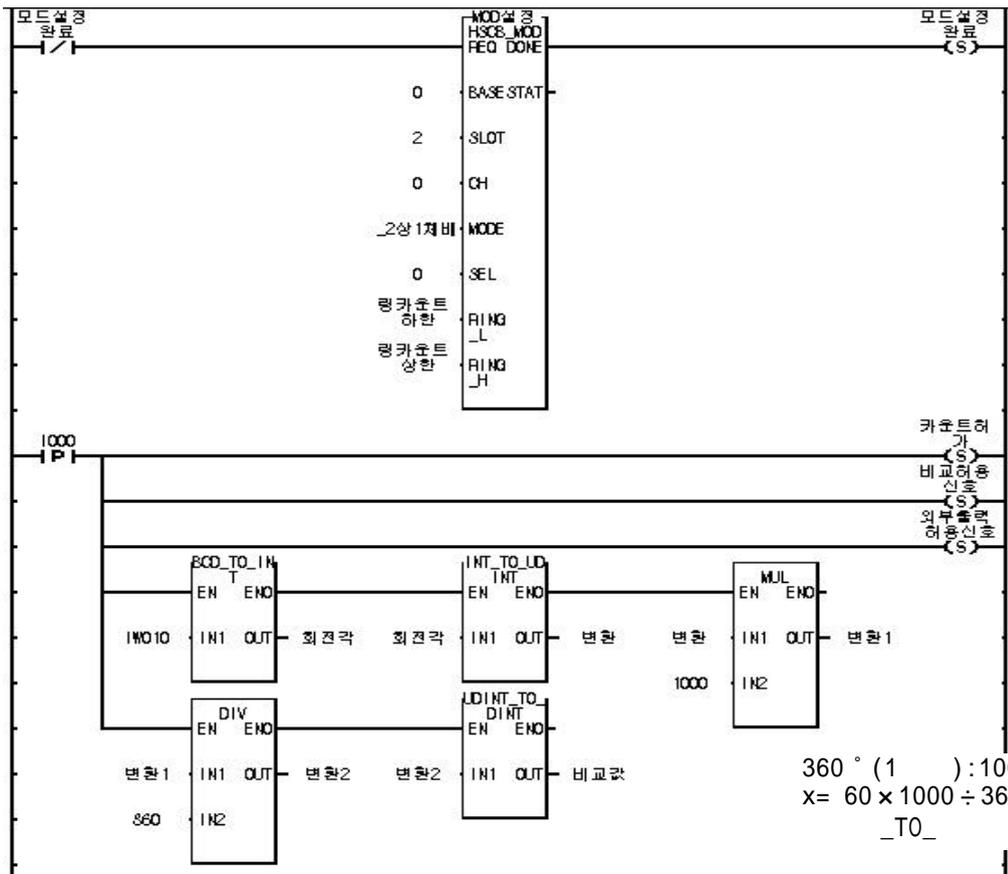
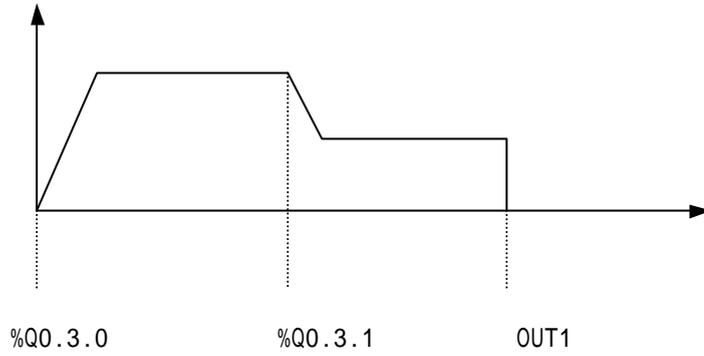


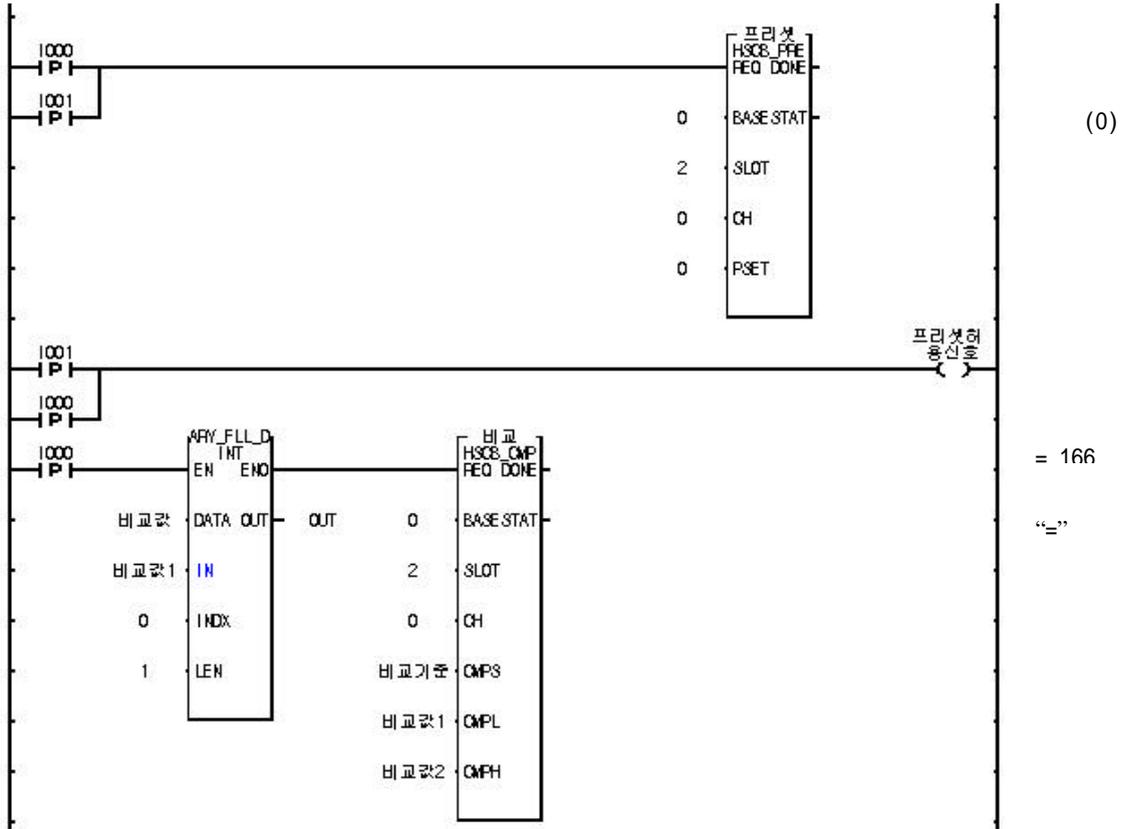
5.3.2



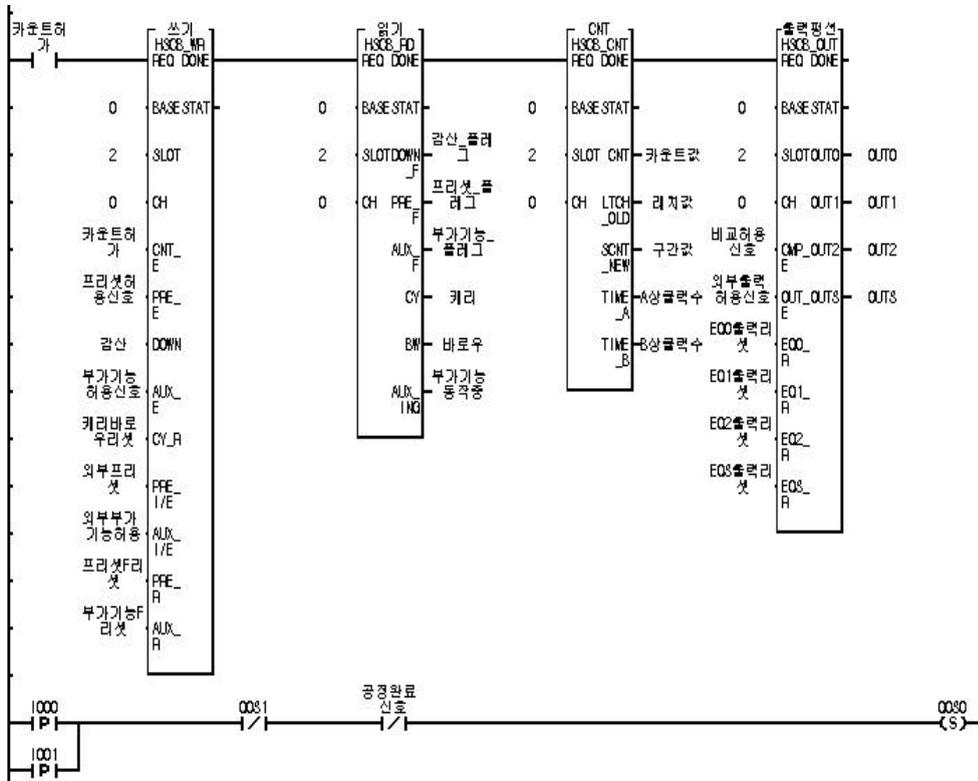
(60°)

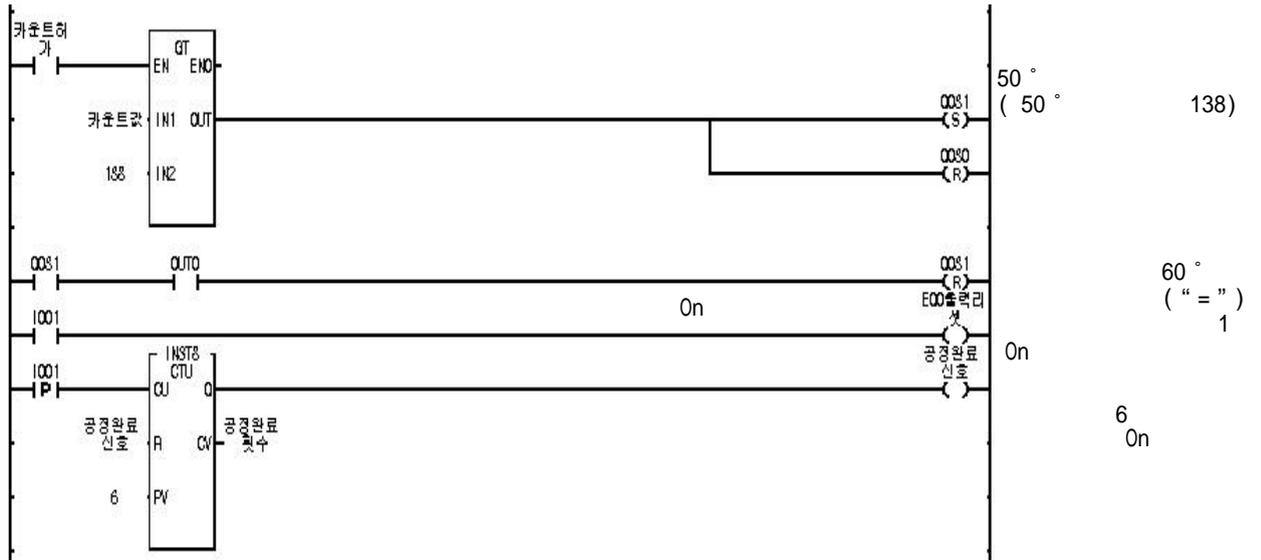
가 On 60°  
6



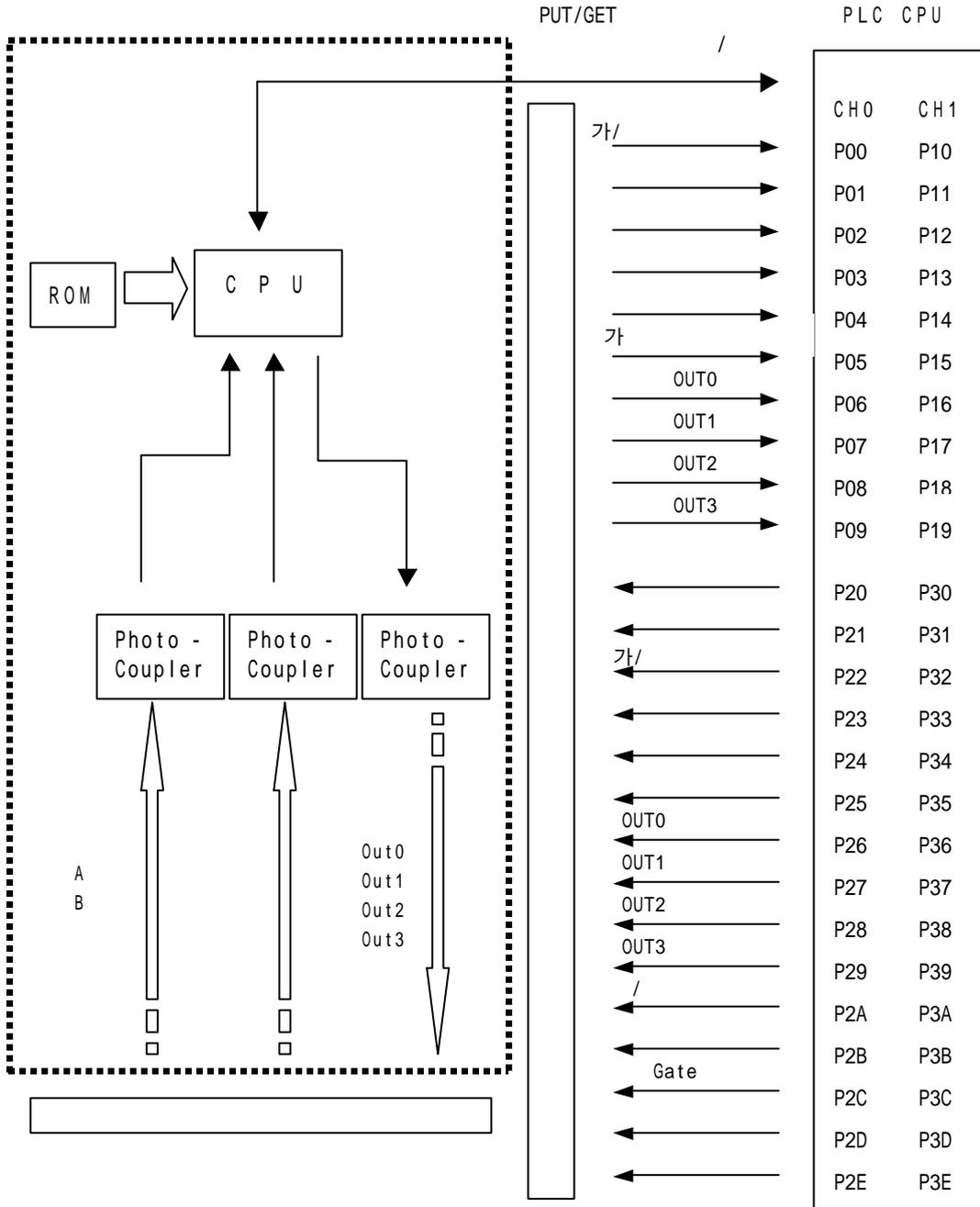


= 166  
“=”





G4F-H01A, G4F-HD1A, G6F-H01A, G6F-HD1A 64



G4F-H01A/HD1A, G6F-H01A/HD1A

6.2

PLC CPU / ( / ) 가 . PLC CPU  
 ( ) PUT, PUTP ( ) GET, GETP  
 .( 7.1 / )

6.2.1

1)

( )		
0	1	
0000	0032	
0001	0033	
0002	0034	가
0003	0035	OUT0
0004	0036	OUT1
0005	0037	OUT2
0006	0038	OUT3
0007	0039	
0008	0040	
0009	0041	(Ring)
0010	0042	
0011	0043	(Ring)
0012	0044	
0013	0045	
0014	0046	-
0015	0047	OUT0 ( )/ ( )
0016	0048	
0017	0049	OUT0 ( )
0018	0050	
0019	0051	OUT1 ( )/ ( )
0020	0052	
0021	0053	OUT1 ( )
0022	0054	
0023	0055	OUT2 ( )/ ( )
0024	0056	
0025	0057	OUT2 ( )
0026	0058	
0027	0059	OUT3 ( )/ ( )
0028	0060	
0029	0061	OUT4 ( )
0030	0062	

2)

( )		
0	1	
64	80	
65	81	
66	82	
67	83	or
68	84	or
69	85	
70	86	A
71	87	
72	88	B
73	89	

6.2.2

1)

(CH0: 0 , CH1: 32 )

( )	
0	2 1
1	2 2
2	2 4
3	CW / CCW
4	1 1 1
5	1 1 2
6	1 2 1
7	1 2 2

2)

(CH0: 1 , CH1: 33 )

( )	
0	Linear
1	Ring

3) 가

(CH0: 2 , CH1: 34 )

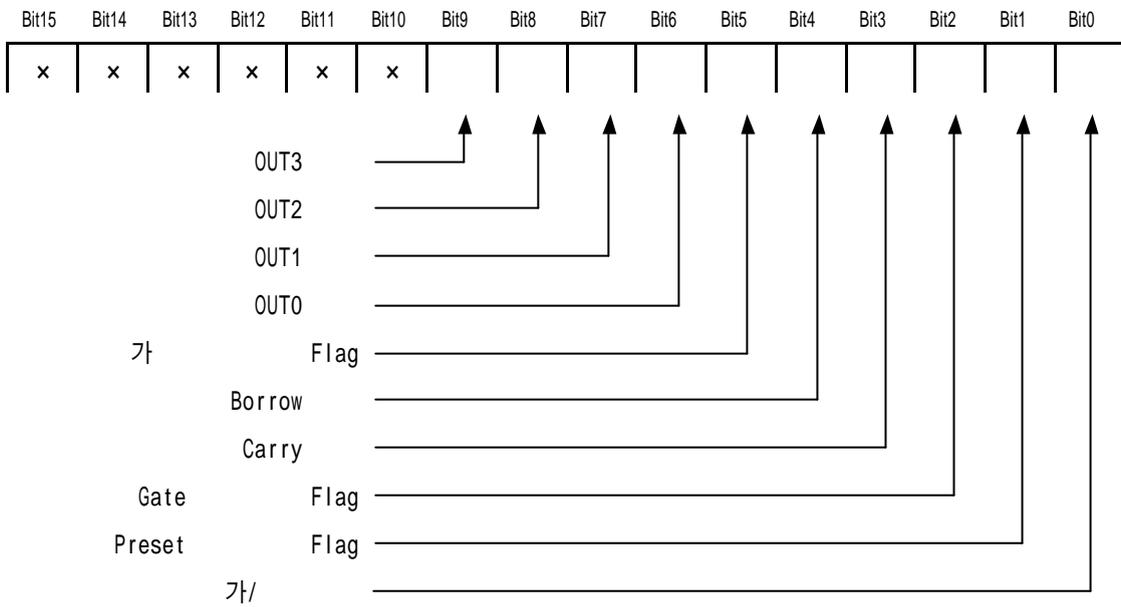
( )	
0	가
1	Clear
2	Latch
3	
4	
5	

4) (CH0: 3 6 , CH1: 35 38 )

	0	1				
OUT0	3	35	0	<	OUT	ON
OUT1	4	36	1	=<	OUT	ON
OUT2	5	37	2	=	OUT	ON
OUT3	6	38	3	>=	OUT	ON
			4	>	OUT	ON
			5	1=<	=<	2 OUT ON
			6	1 >=	,	>= 2 OUT ON

6.2.3

0 : 76 , 1 : 77



6.3

G4F-H01A, G4F-HD1A, G6F-H01A, G6F-HD1A 64

PLC <-			PLC ->		
0	P(N)0	가/ (ON: )	0	P(N+2)0	(Level)
	P(N)1			P(N+2)1	(Edge)
	P(N)2			P(N+2)2	가/ (Level)
	P(N)3			P(N+2)3	(Edge, Level)
	P(N)4			P(N+2)4	(Level)
	P(N)5	가		P(N+2)5	(Level)
	P(N)6	OUT0		P(N+2)6	OUT0 (Edge)
	P(N)7	OUT1		P(N+2)7	OUT1 (Edge)
	P(N)8	OUT2		P(N+2)8	OUT2 (Edge)
	P(N)9	OUT3		P(N+2)9	OUT3 (Edge)
	P(N)A	-		P(N+2)A	/ (Edge)
	P(N)B	-		P(N+2)B	
	P(N)C	-		P(N+2)C	
	P(N)D	-		P(N+2)D	
	P(N)E	-		P(N+2)E	
	P(N)F	-		P(N+2)F	-
1	P(N+1)0	가/ (ON: )	1	P(N+3)0	(Level)
	P(N+1)1			P(N+3)1	(Edge)
	P(N+1)2			P(N+3)2	가/ (Level)
	P(N+1)3			P(N+3)3	(Edge, Level)
	P(N+1)4			P(N+3)4	(Level)
	P(N+1)5	가		P(N+3)5	(Level)
	P(N+1)6	OUT0		P(N+3)6	OUT0 (Edge)
	P(N+1)7	OUT1		P(N+3)7	OUT1 (Edge)
	P(N+1)8	OUT2		P(N+3)8	OUT2 (Edge)
	P(N+1)9	OUT3		P(N+3)9	OUT3 (Edge)
	P(N+1)A	-		P(N+3)A	/ (Edge)
	P(N+1)B	-		P(N+3)B	
	P(N+1)C	-		P(N+3)C	
	P(N+1)D	-		P(N+3)D	
	P(N+1)E	-		P(N+3)E	
	P(N+1)F	-		P(N+3)F	-

' N ' /

7.1 /

PLC CPU

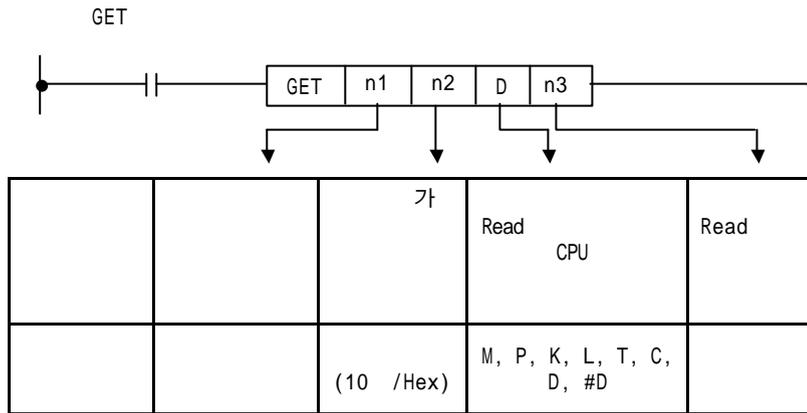
7.1.1

Read PLC CPU ( )

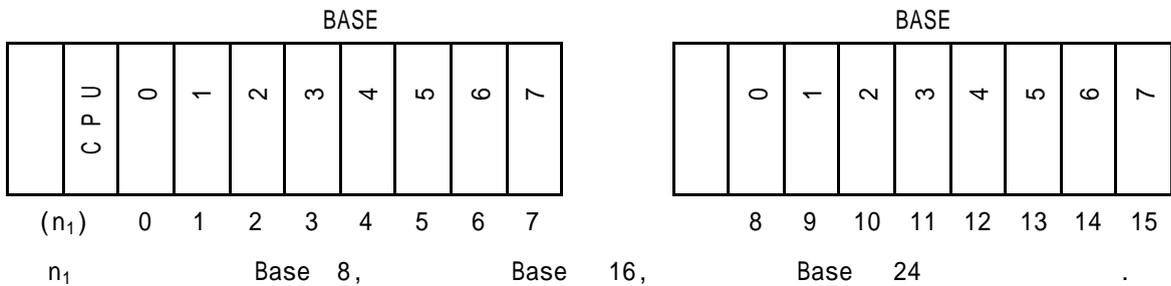
1) GET/GETP

On	(  )	GET
	(  )	GETP

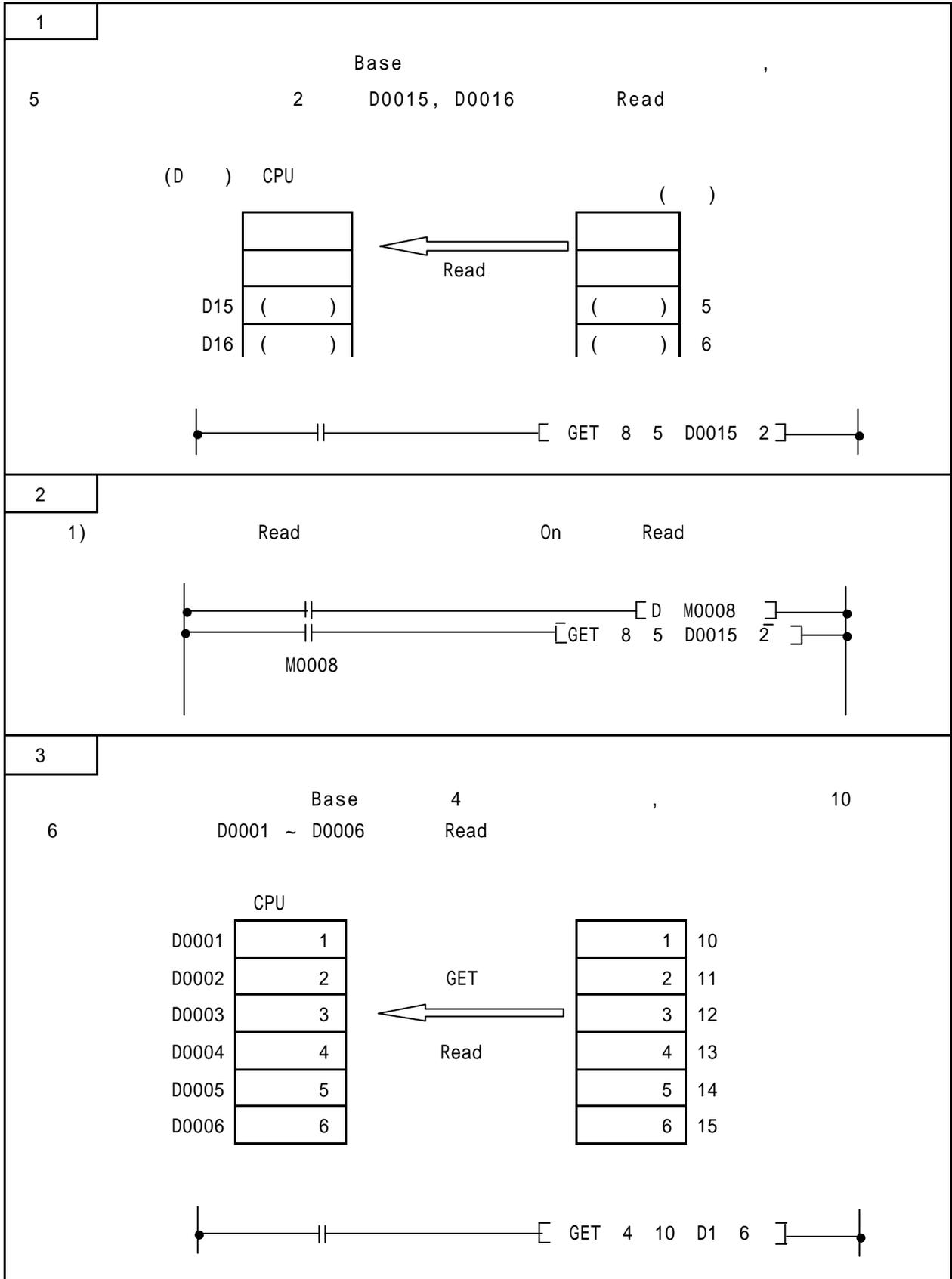
2) GET/GETP



3) n1( )

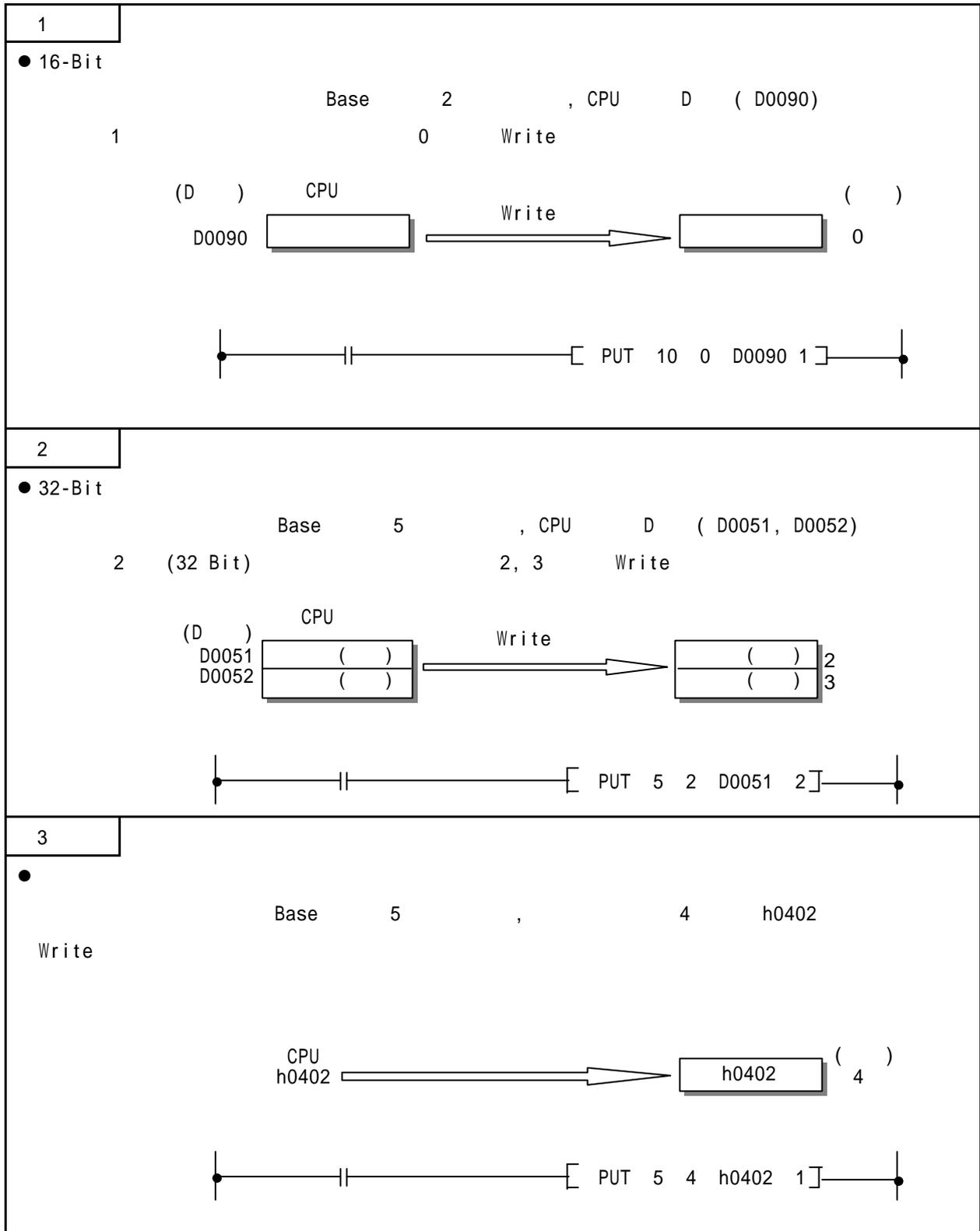


4) GET/GETP





4) PUT/PUTP



3

7.2

2

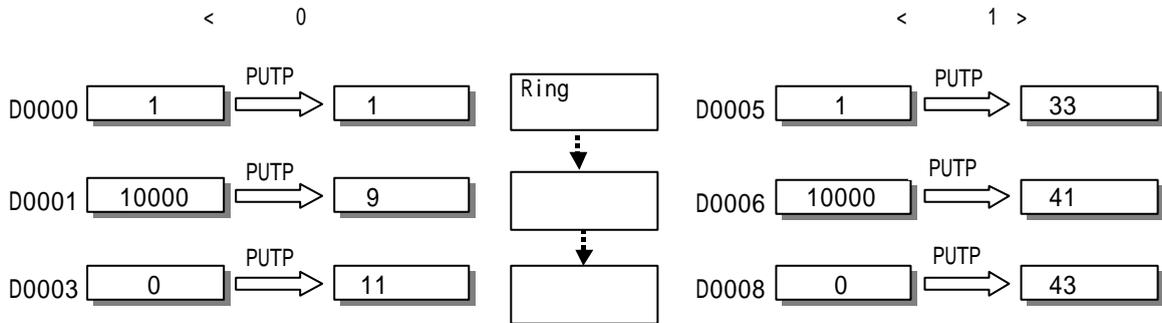
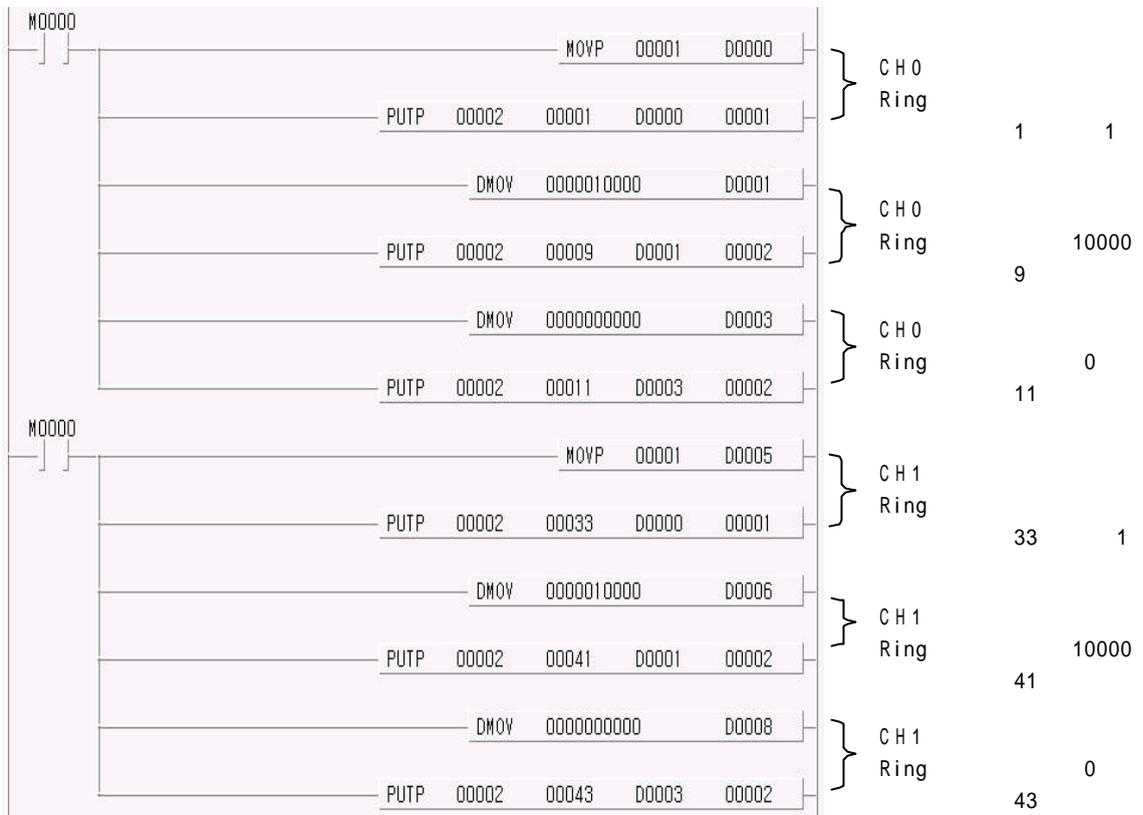
G4F-H01A

GM4-PA2A	K4P-15AS CPU	G4I-D22A 0	G4Q-RY2A 1	G4F-H01A 2	G4Q-TR2A 3
		P00	P01	P02 P03 P04 P05	P06

}

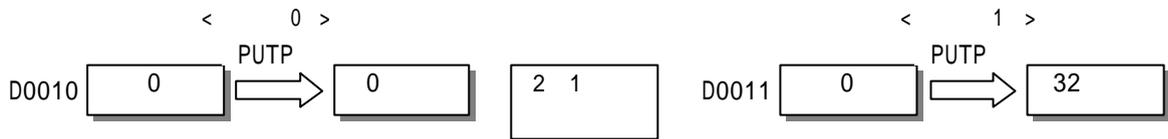
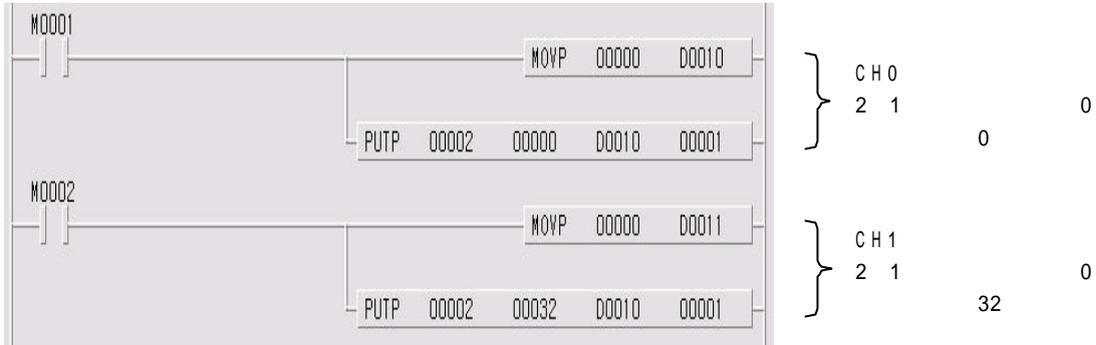
7.2.1

, Linear , Ring

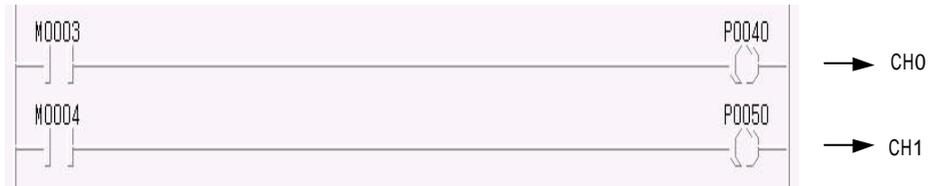


7.2.2

2 1 , 2 2 , 2 4 , CW/CCW, 1 1 1 1, 1 1 2 , 1 2 1 ,  
 1 2 2 가 ,  
 2 1 , 2 1 .

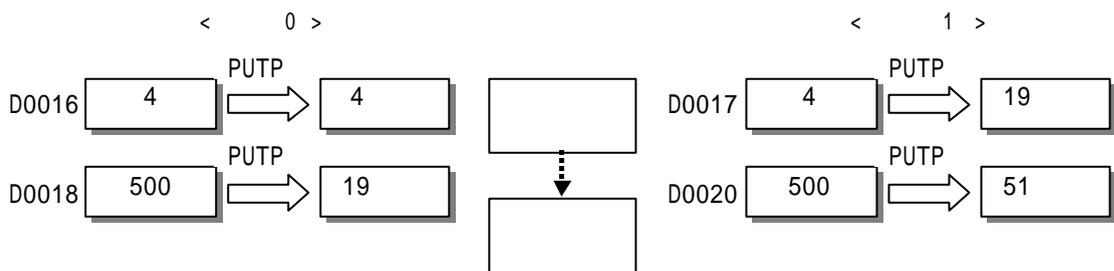
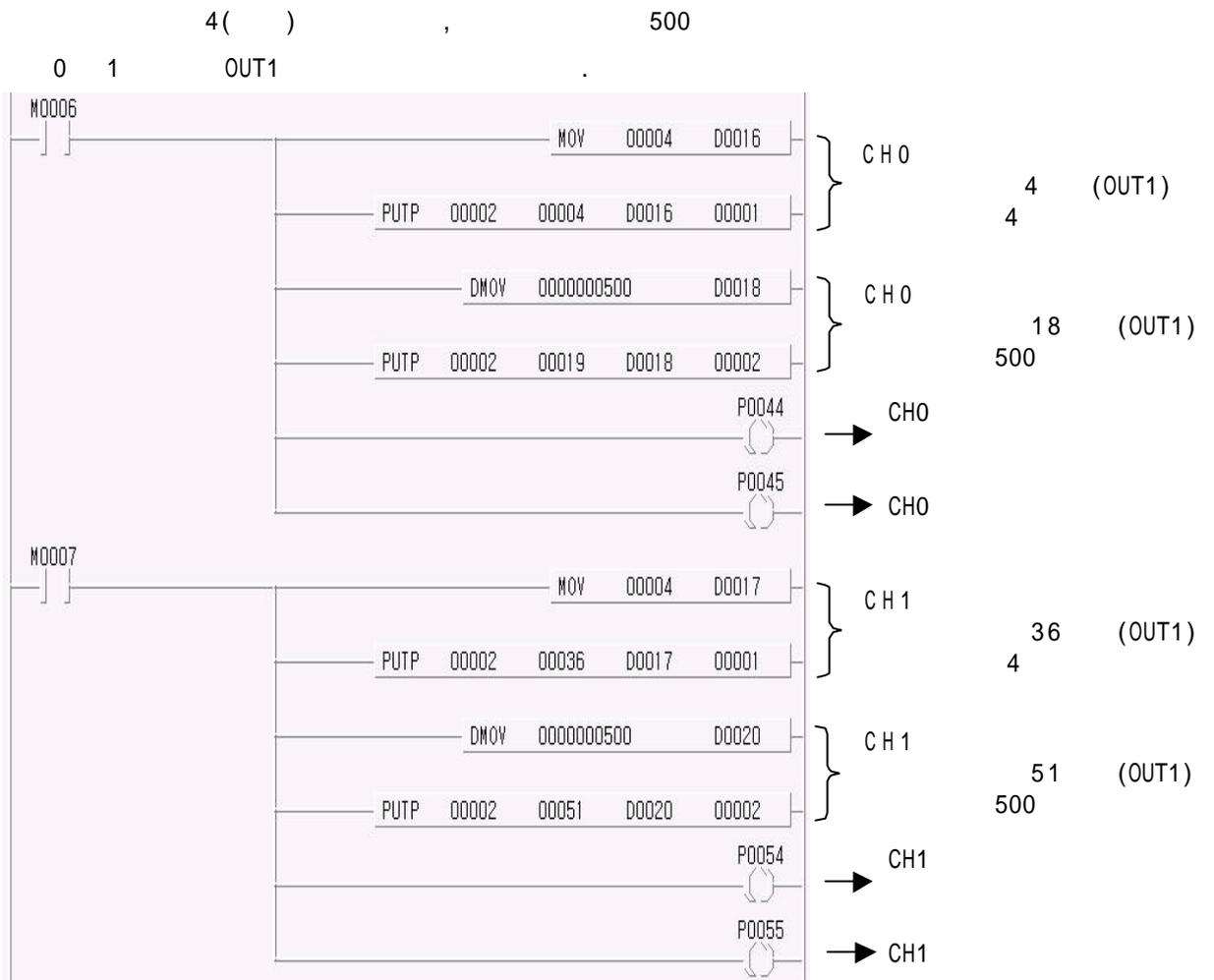


7.2.3

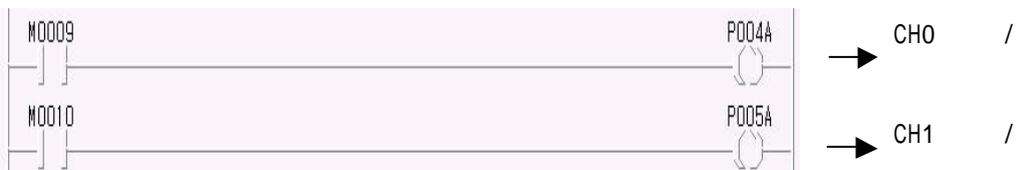




7.2.6

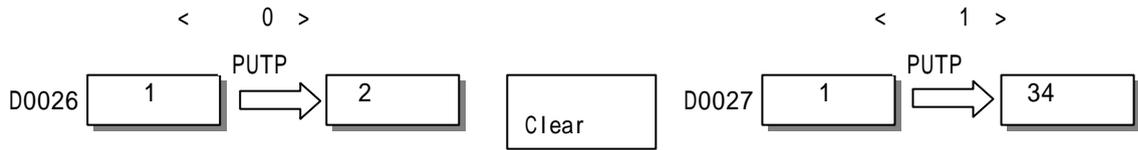
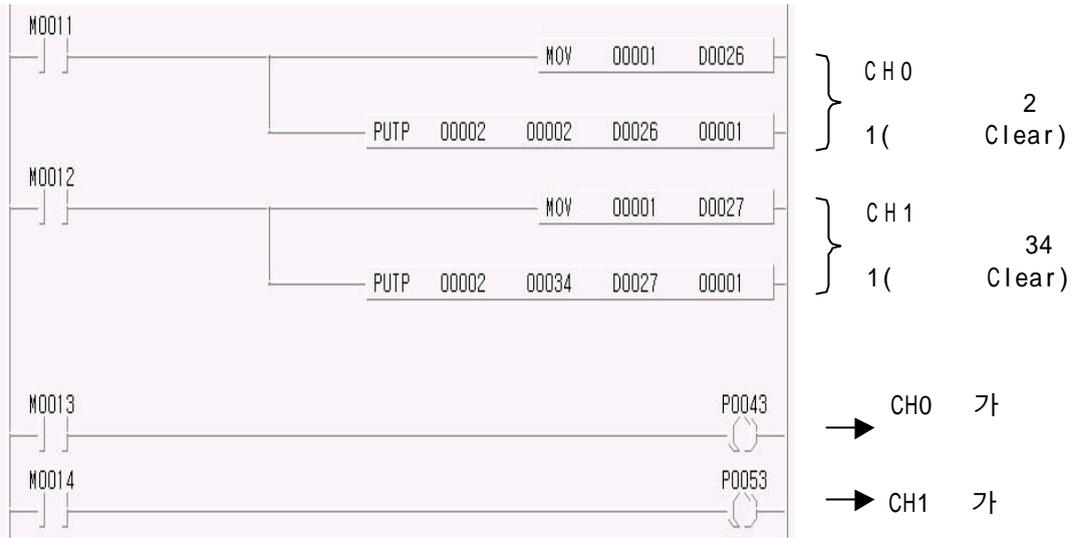


7.2.7 /

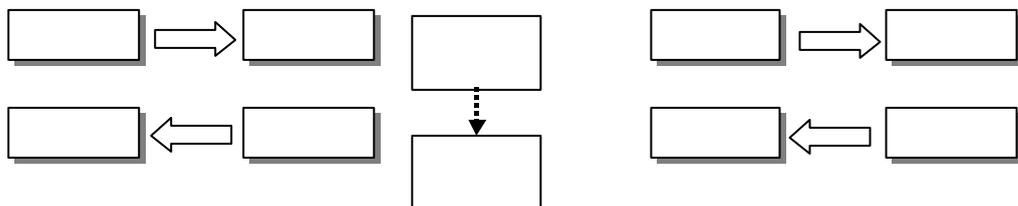
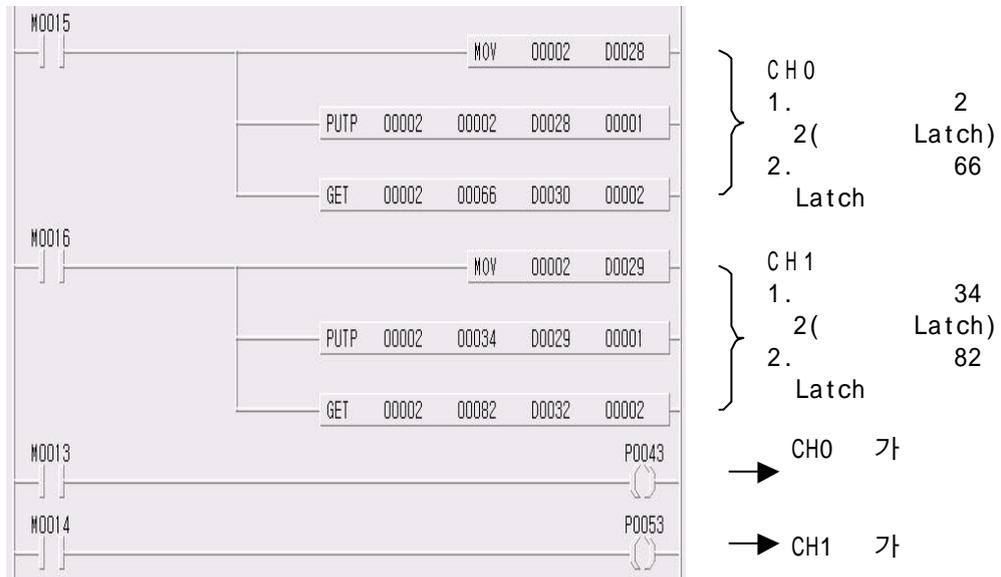


7.2.8 가

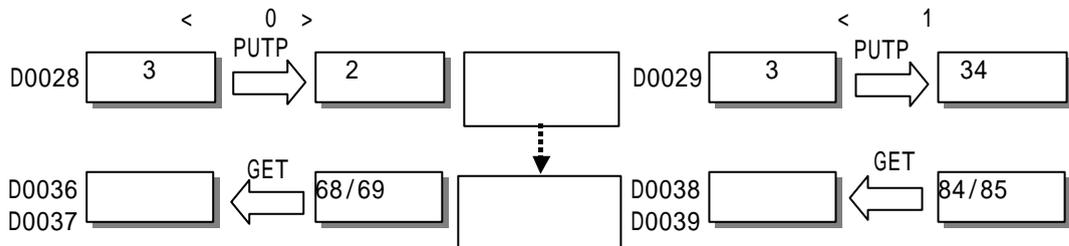
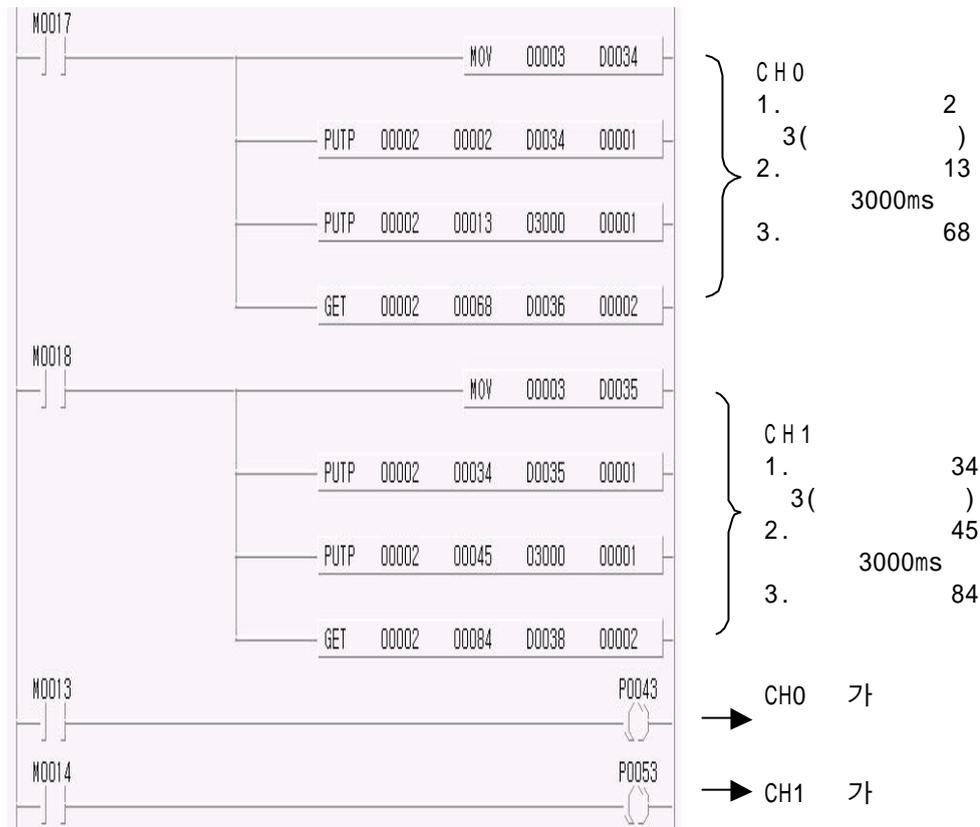
1)



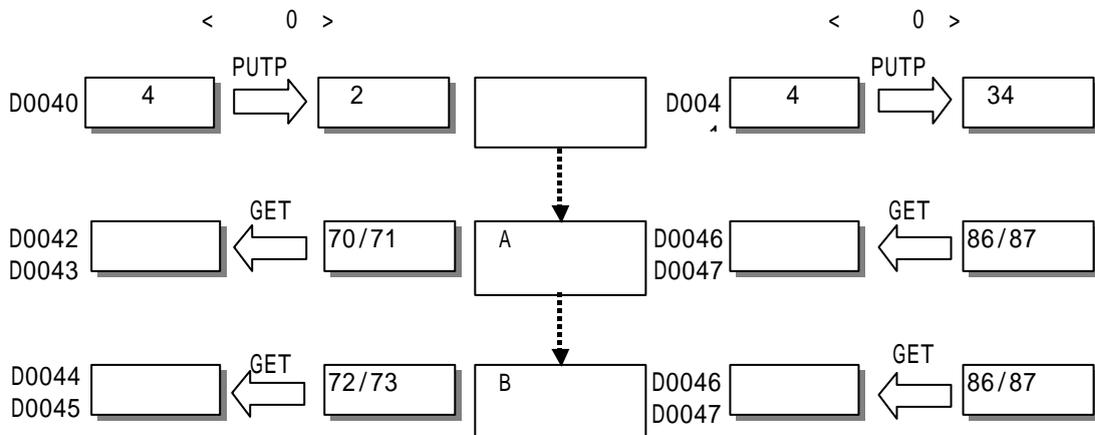
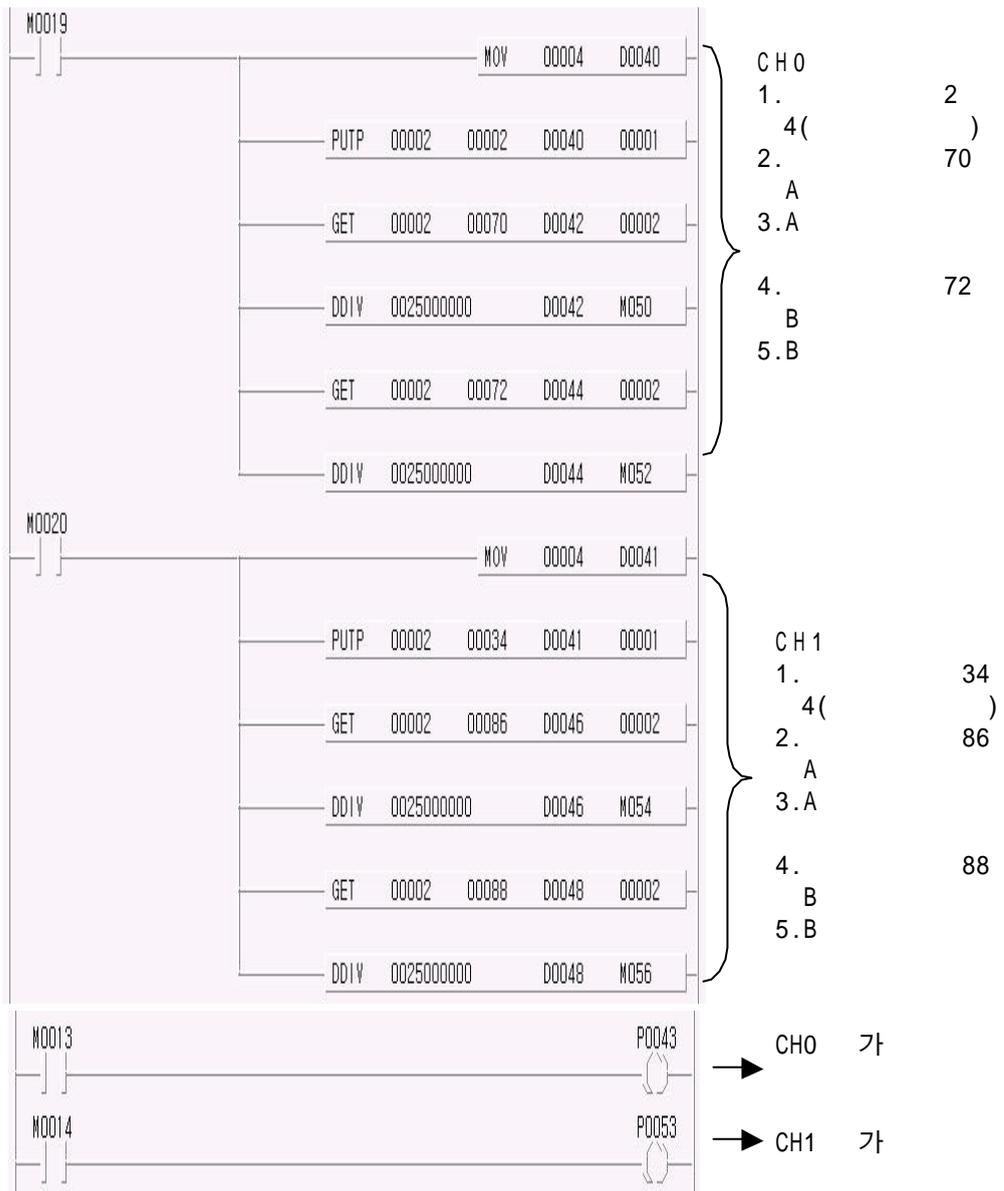
2)



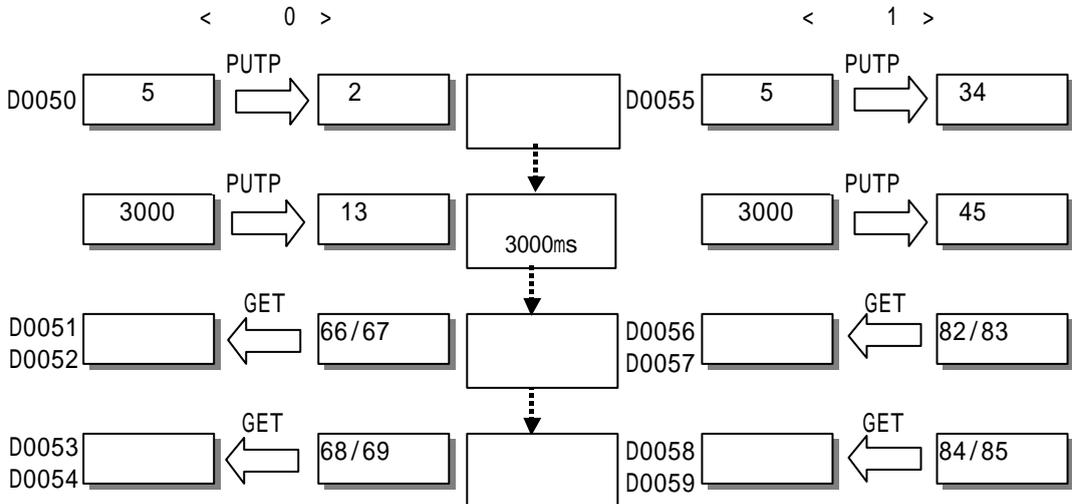
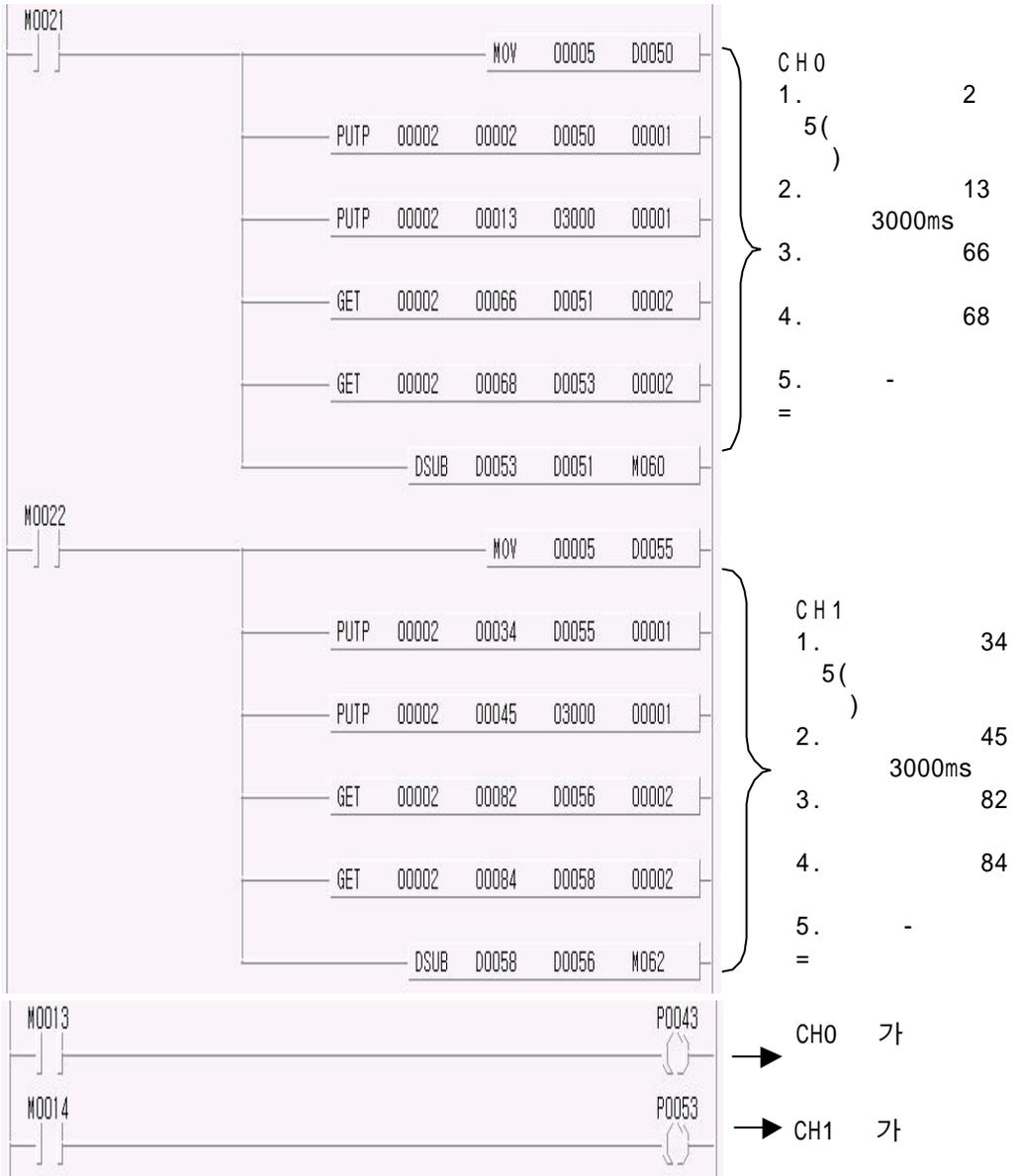
3)



4)

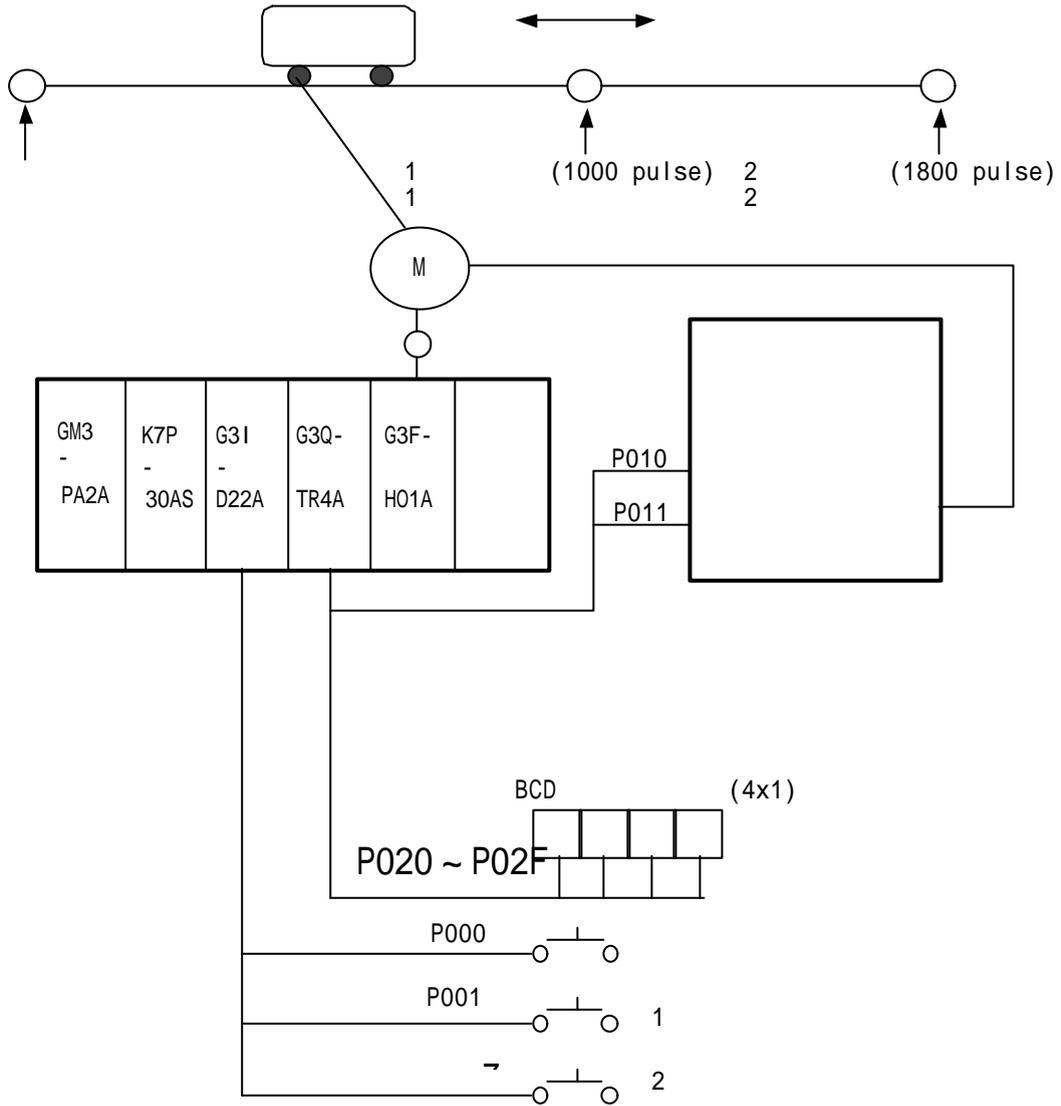


5)



7.3

7.3.1

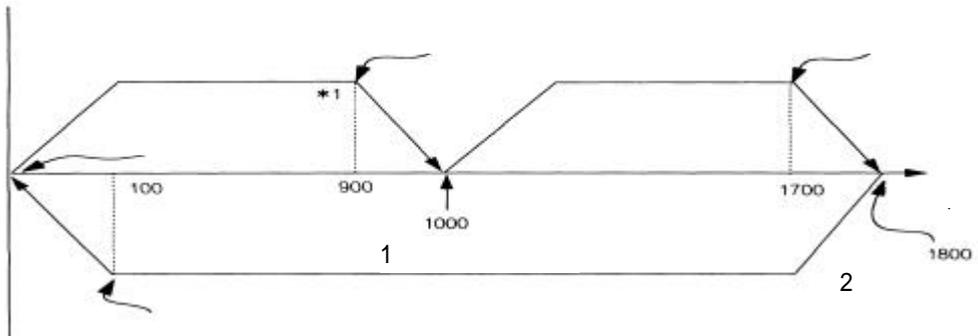


가

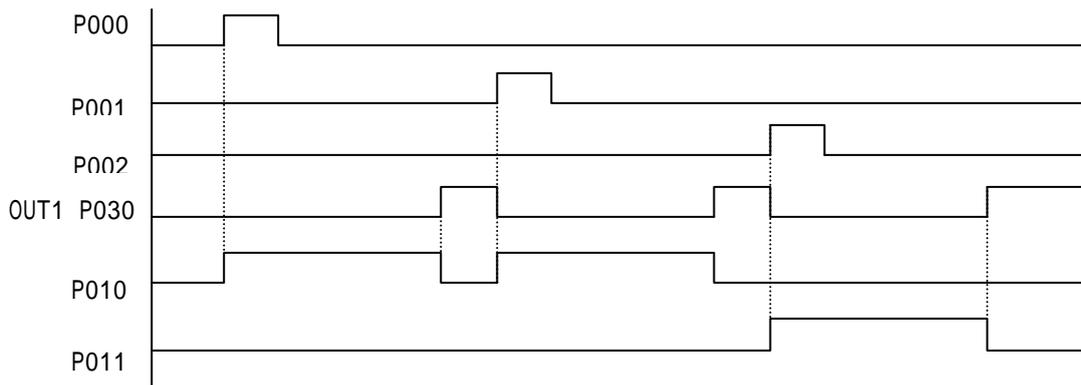
1  
 1 가 On 2  
 가 On . 2

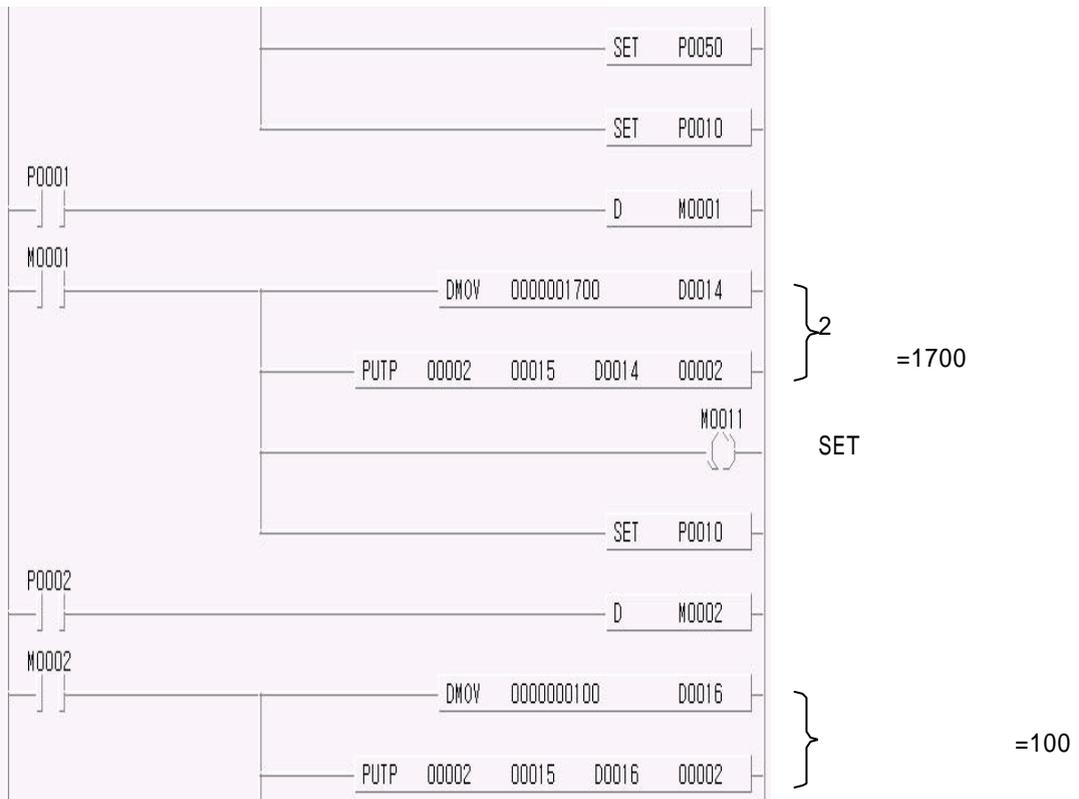
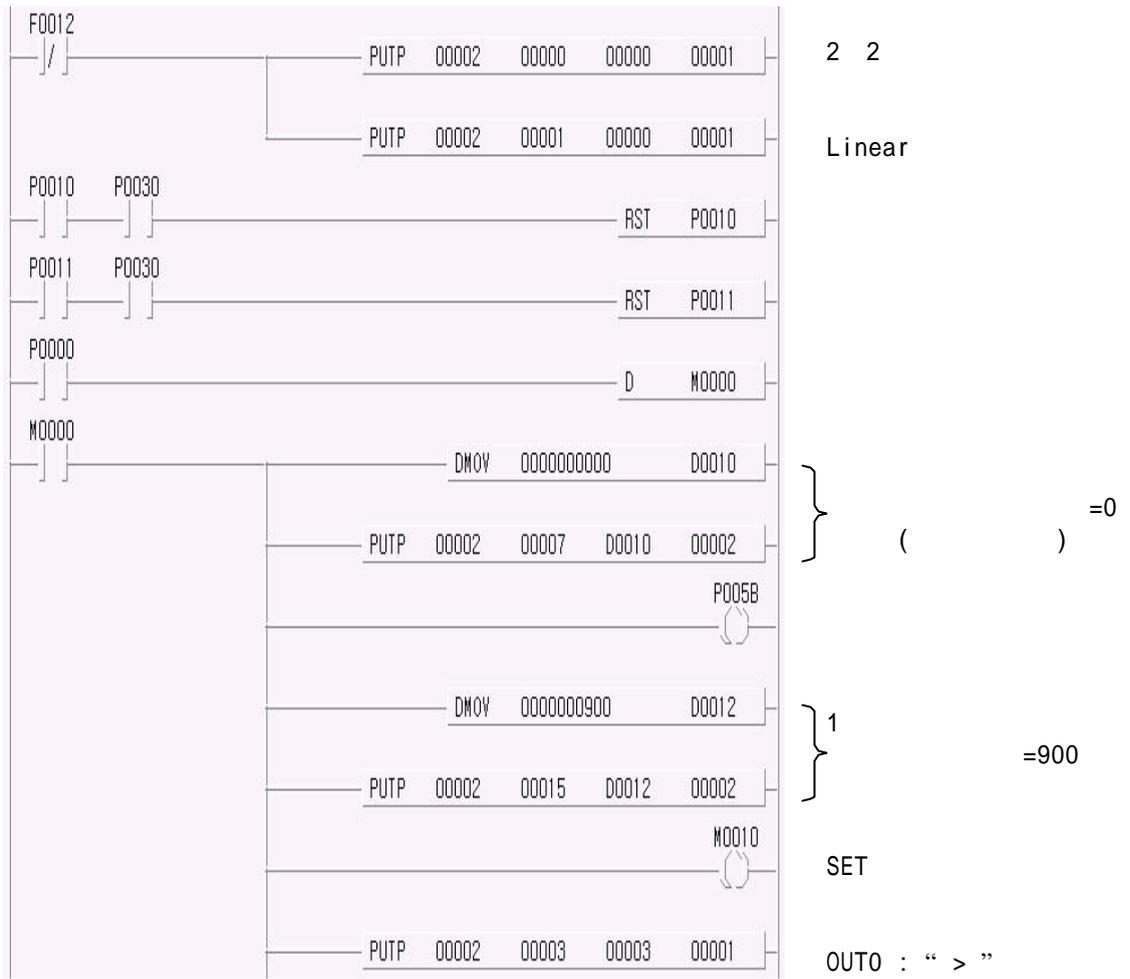
/  
 P000 :  
 P001 : 1 }  
 P002 : 2 }  
 P010 : (On : , Off : ) }  
 P011 : (On : , Off : ) }  
 P020 ~ P02F : (BCD)  
 P030 ~ P04F :  
 P050 ~ P06F :

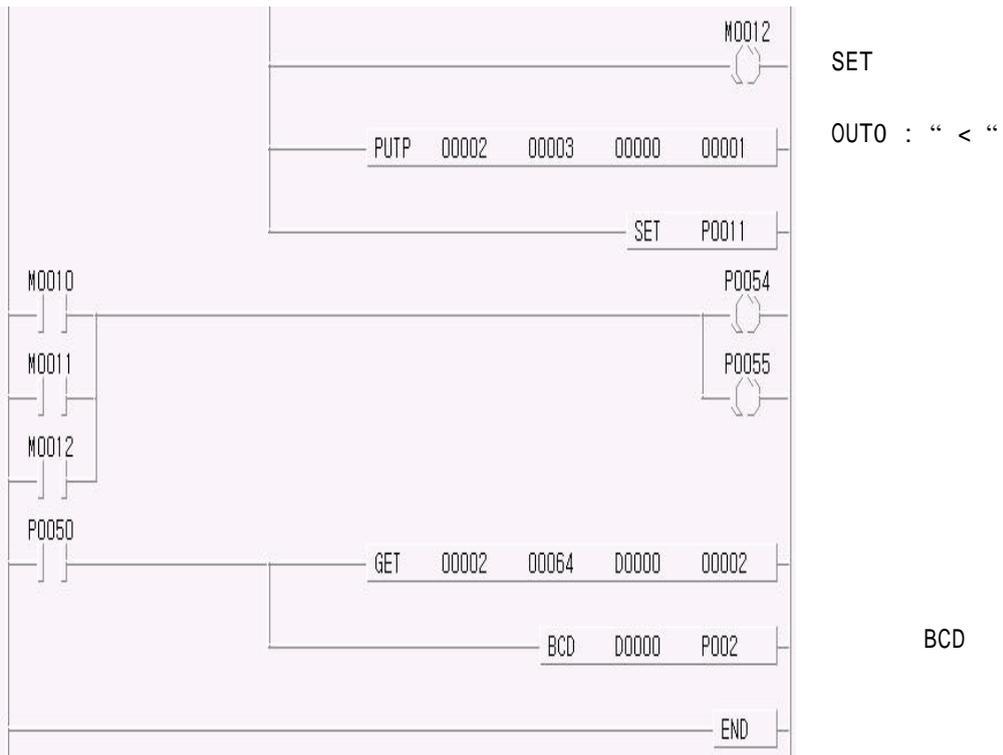
D  
 D0000 ~ D0001 :



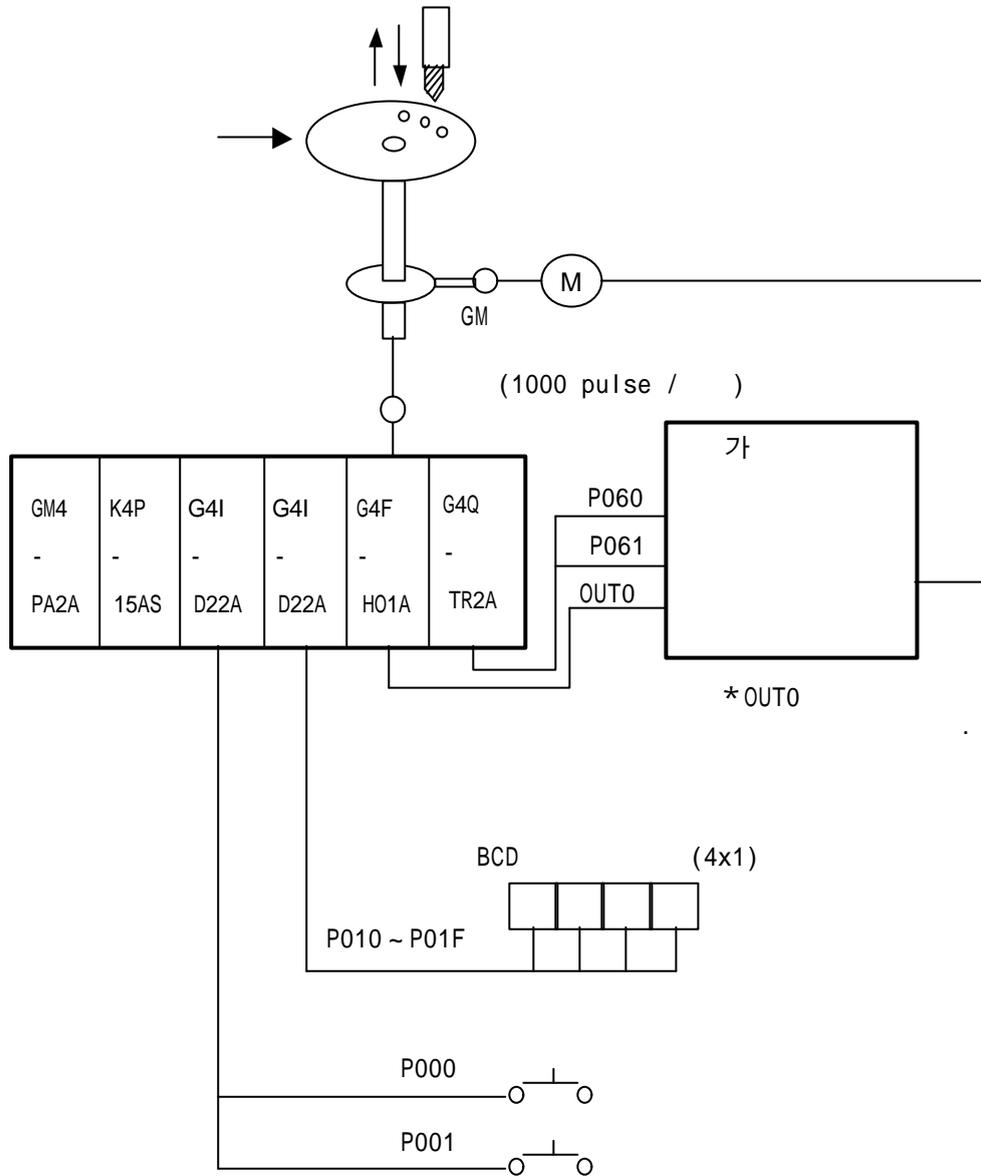
\*1: 100







7.3.2



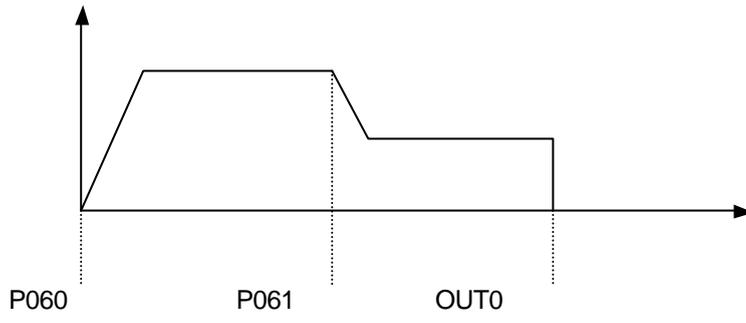
K4P-15AS : MK300S CPU

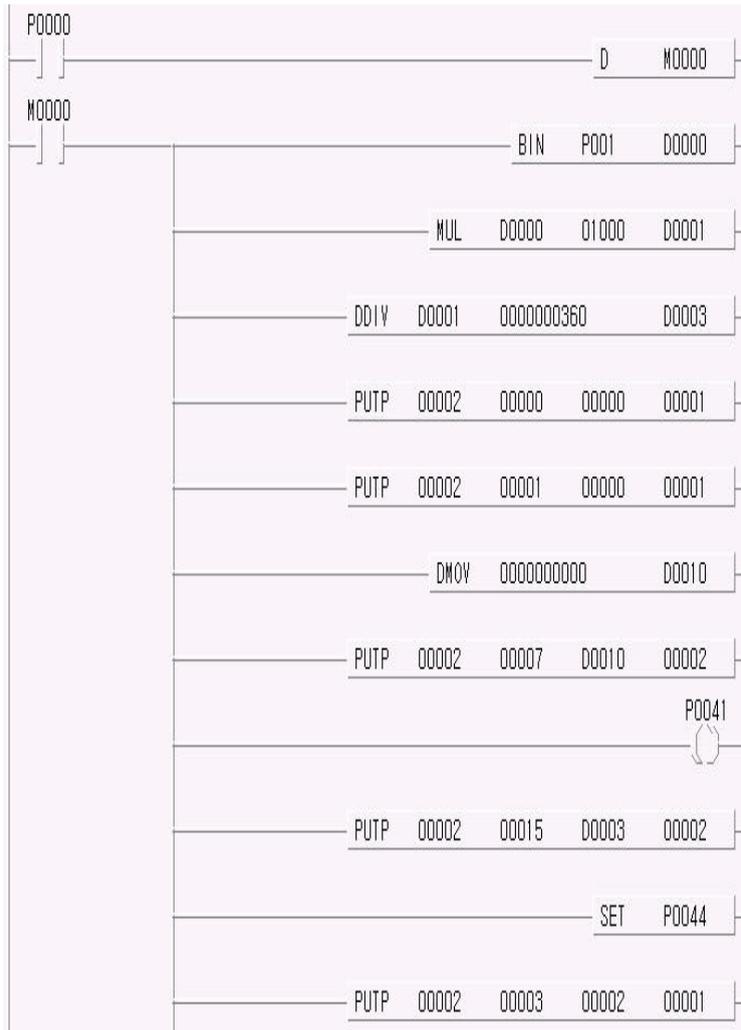
G4I-D22A : DC (16 )

G4F-H01A : (64 )

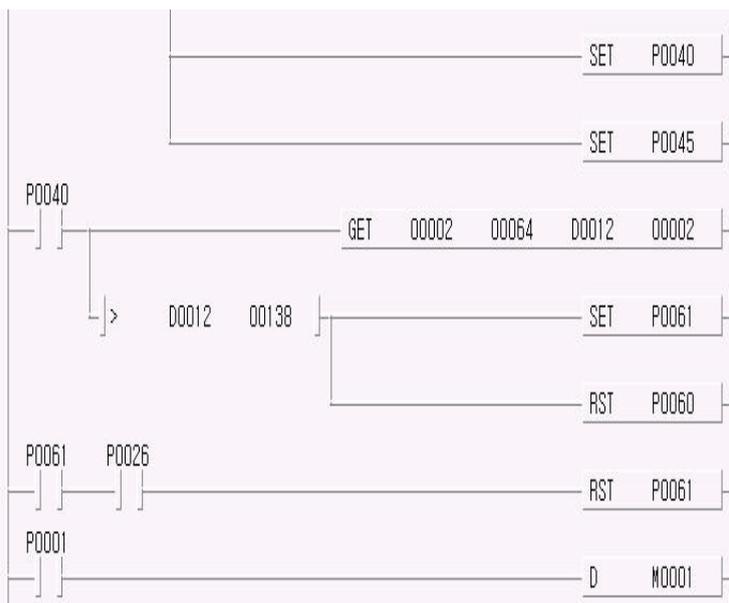
G4Q-TR2A : TR (16 )

6 가 On 60° (60°)

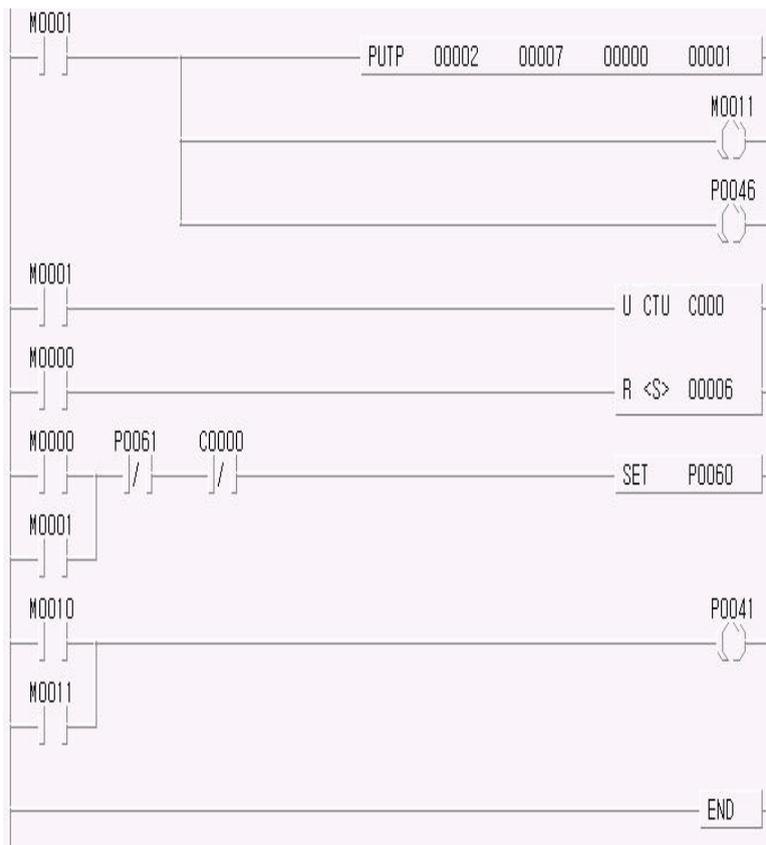




1 On  
 BIN 60 BCD  
 $360:1000 = 60:X$   
 $X = D3 = 166$   
 2 1  
 Linear  
 } = 0  
 =166



D0010, D0011



8

CPU

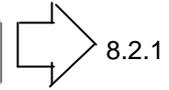
CPU

8.1

8.1.1

LED

READY LED가

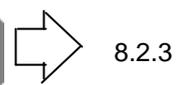


8.1.2

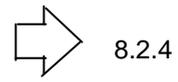
가



가

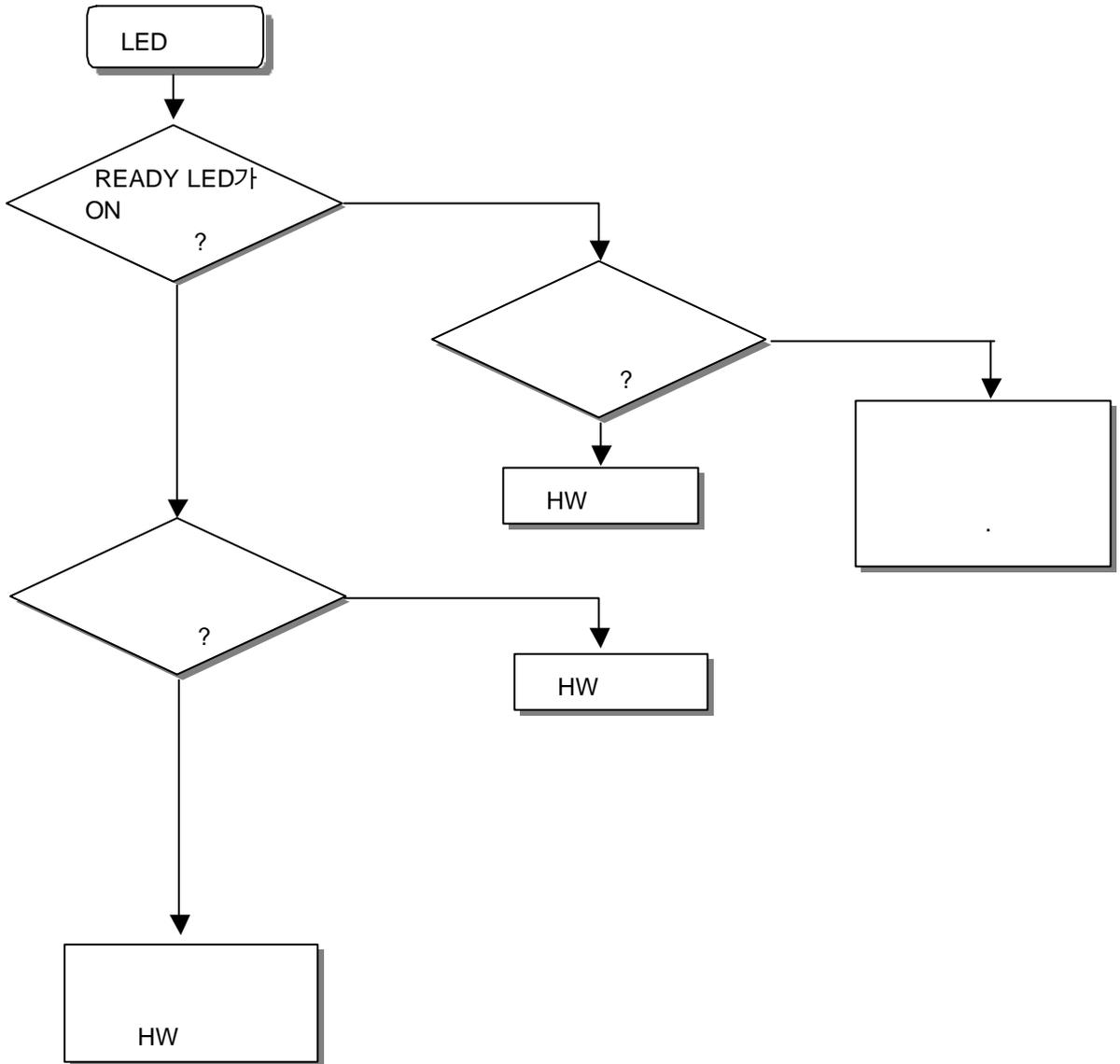


8.1.3

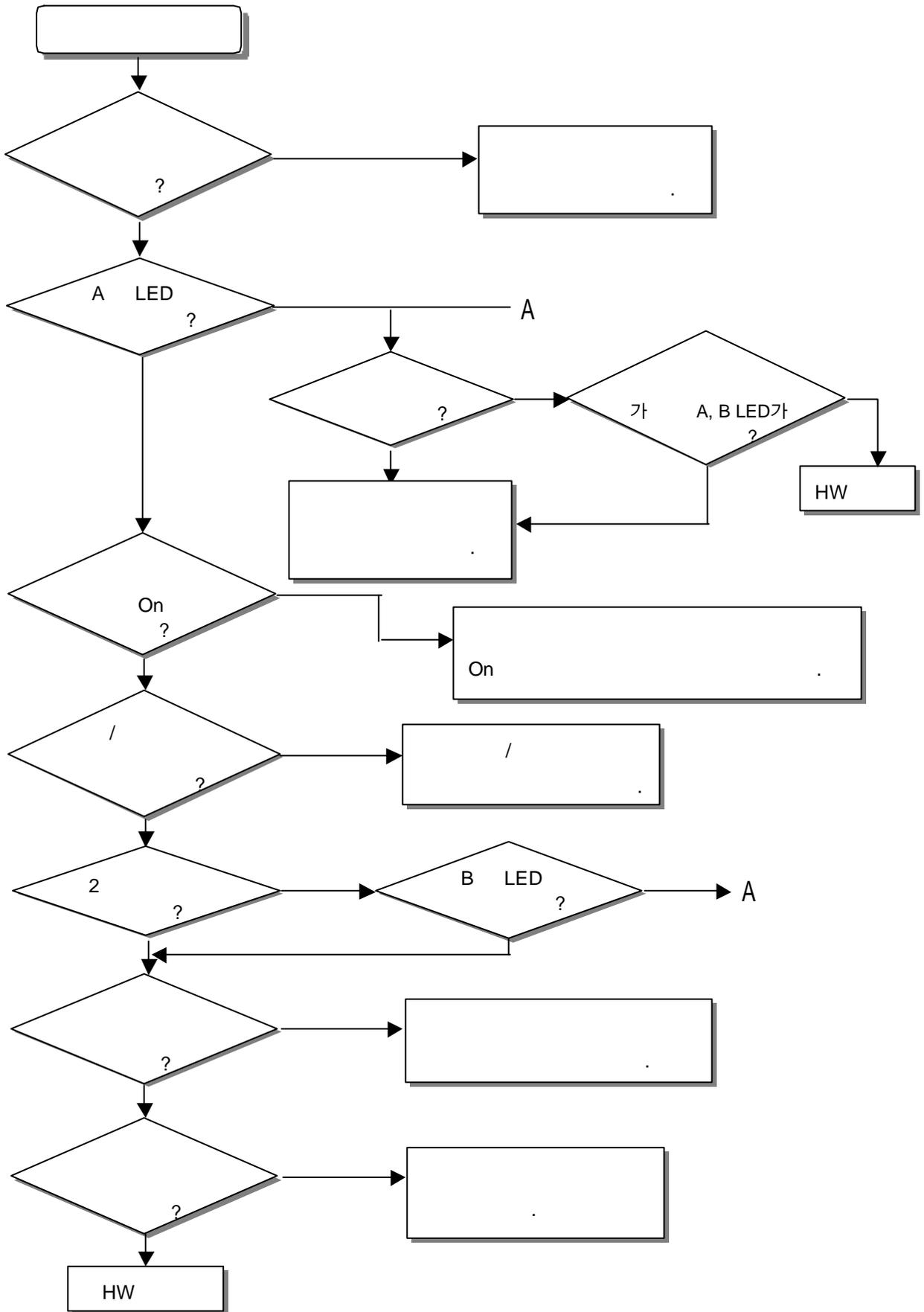


8.2

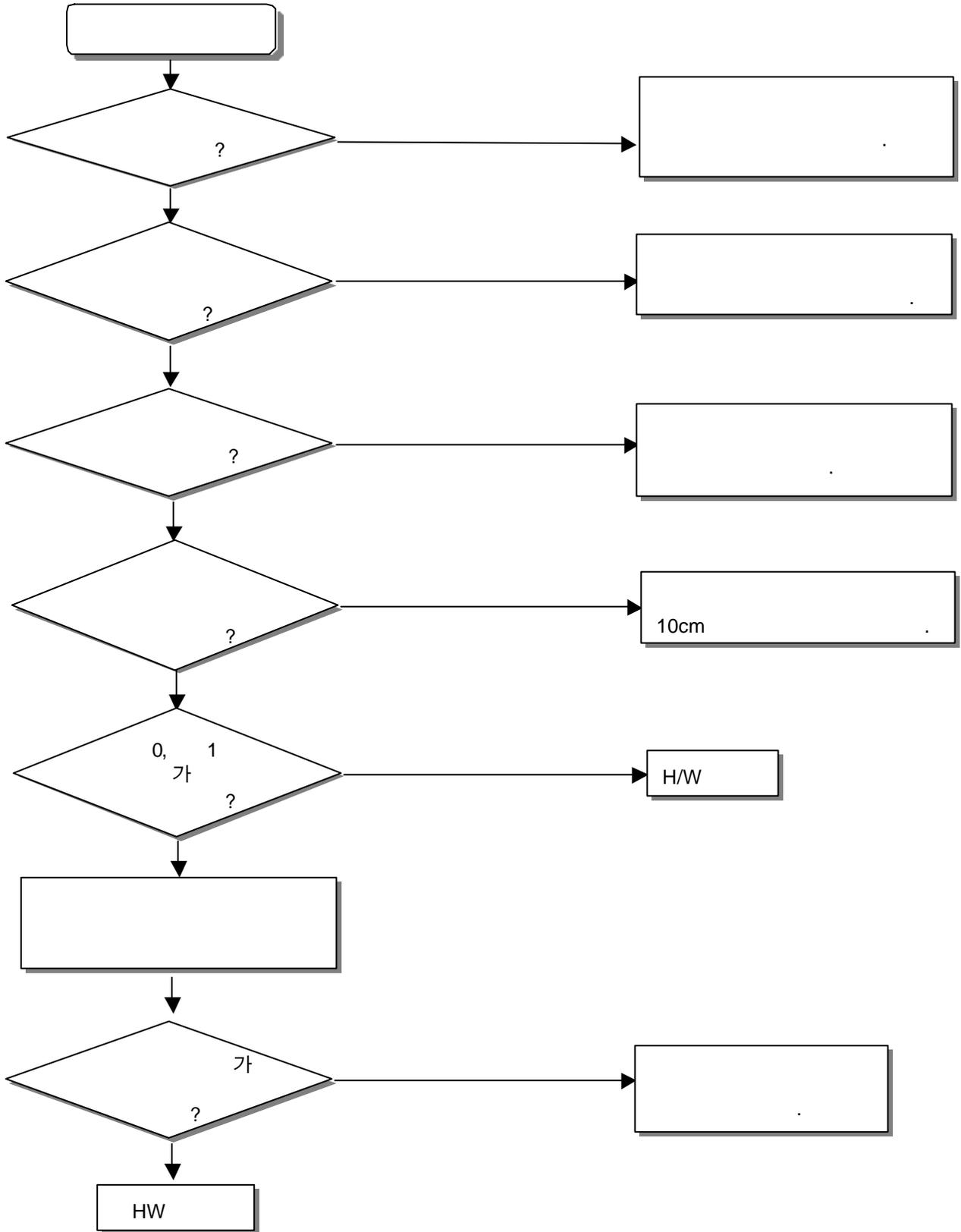
8.2.1 LED



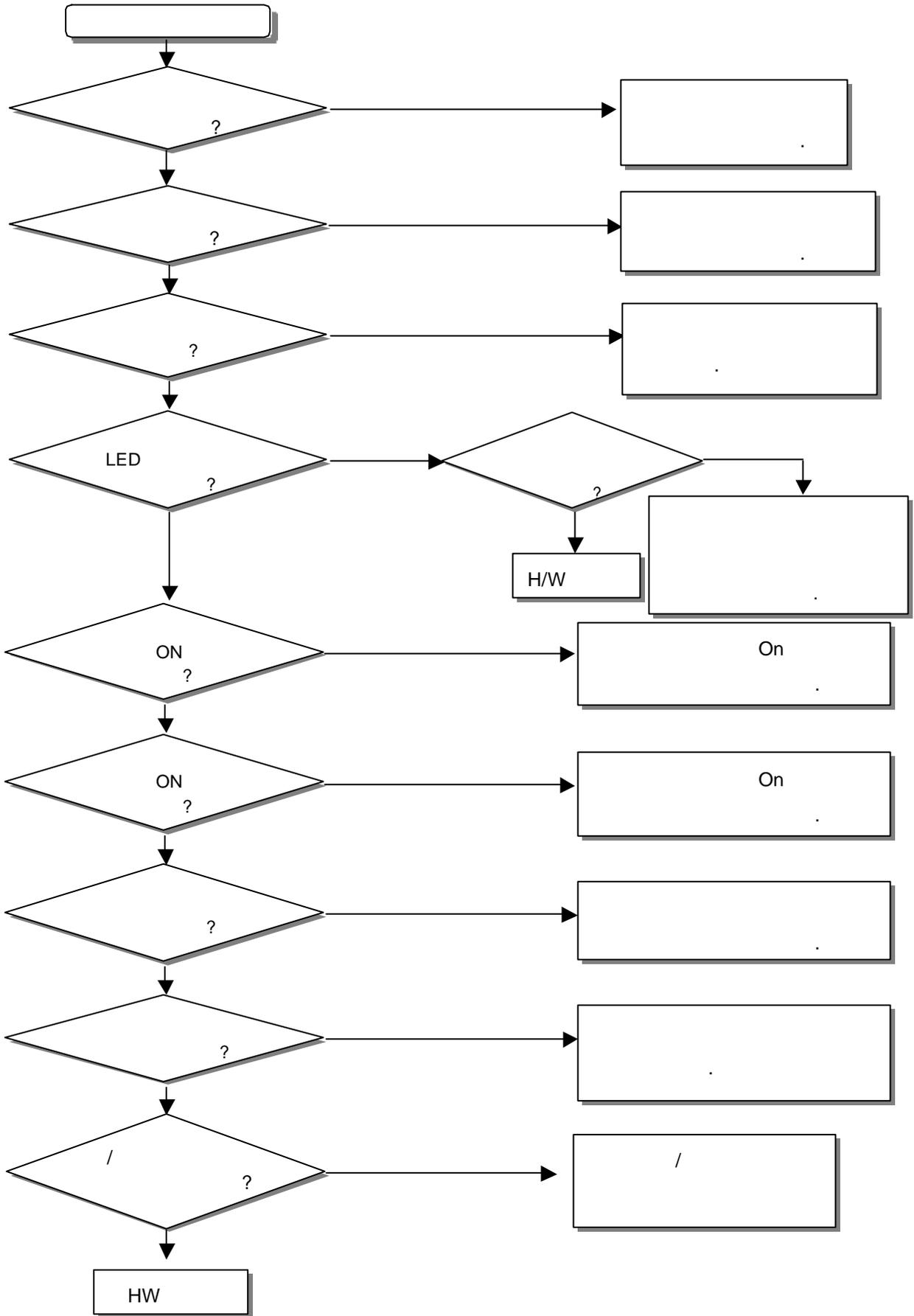
8.2.2



8.2.3



8.2.4



1  
 1 1 1 ..... 2-7  
 1 1 2 ..... 2-8  
 1 2 1 ..... 2-8  
 1 2 2 ..... 2-8  
  
 2  
 2 1 ..... 2-9  
 2 ..... 2-9  
  
 ㄱ  
 ..... 2-21,5-13,7-11  
  
 ㄴ  
 ..... 6-2  
 ..... 7-3  
 ..... 7-1  
  
 ㄷ  
 ..... 2-23,5-15,7-13  
 ..... 6-3  
  
 ㄹ  
 (Linear) ..... 2-11  
 (Ring) ..... 2-12  
 ..... 3-5  
 ..... 5-3  
  
 ㅁ  
 0 ..... 2-14  
 1 ..... 2-15  
 2 ..... 2-15  
 3 ..... 2-16  
 4 ..... 2-16  
 5 ..... 2-17

6 ..... 2-17  
  
 ㅂ  
 (Borrow) ..... 2-18  
 가 ..... 2-19,5-11  
 가 ..... 6-3  
 가 ..... 4-4,4-12,7-10  
 ..... 4-5, 4-13  
 ..... 2-14,4-9, 4-17  
 ..... 5-7  
 ..... 5-7,6-4  
 ..... 7-9  
  
 ㅅ  
 ..... 6-4  
  
 ㅇ  
 ..... 2-22  
 ..... 4-18  
 ..... 4-15  
 ..... 4-8, 4-16  
 ..... 4-3, 4-11,7-7  
 ..... 5-14,7-12  
 ..... 6-3  
  
 ㅈ  
 ..... 4-2, 4-10  
  
 ㅋ  
 ..... 2-20,5-12,7-10  
 ..... 2-7  
 ..... 2-19,5-11,7-10  
 (Carry) ..... 2-18  
 ..... 4-6, 4-14  
 / ..... 5-9,7-9  
 ..... 6-3,7-6

**A**

---

..... 7-7

**II**

..... 5-5,7-8

**š**

..... 7-8

**C**

CW(Clockwise)/CCW(Counter Clockwise) ..... 2-10

**D**

DC12V NPN ..... 3-3

DC24V PNP ..... 3-4

DC5V ..... 3-2

**G**

GET/GETP..... 7-1, 7-2

**P**

PUT/PUTP..... 7-3

**R**

RPM ..... 5-2