

LG

Fnet(Fieldbus)

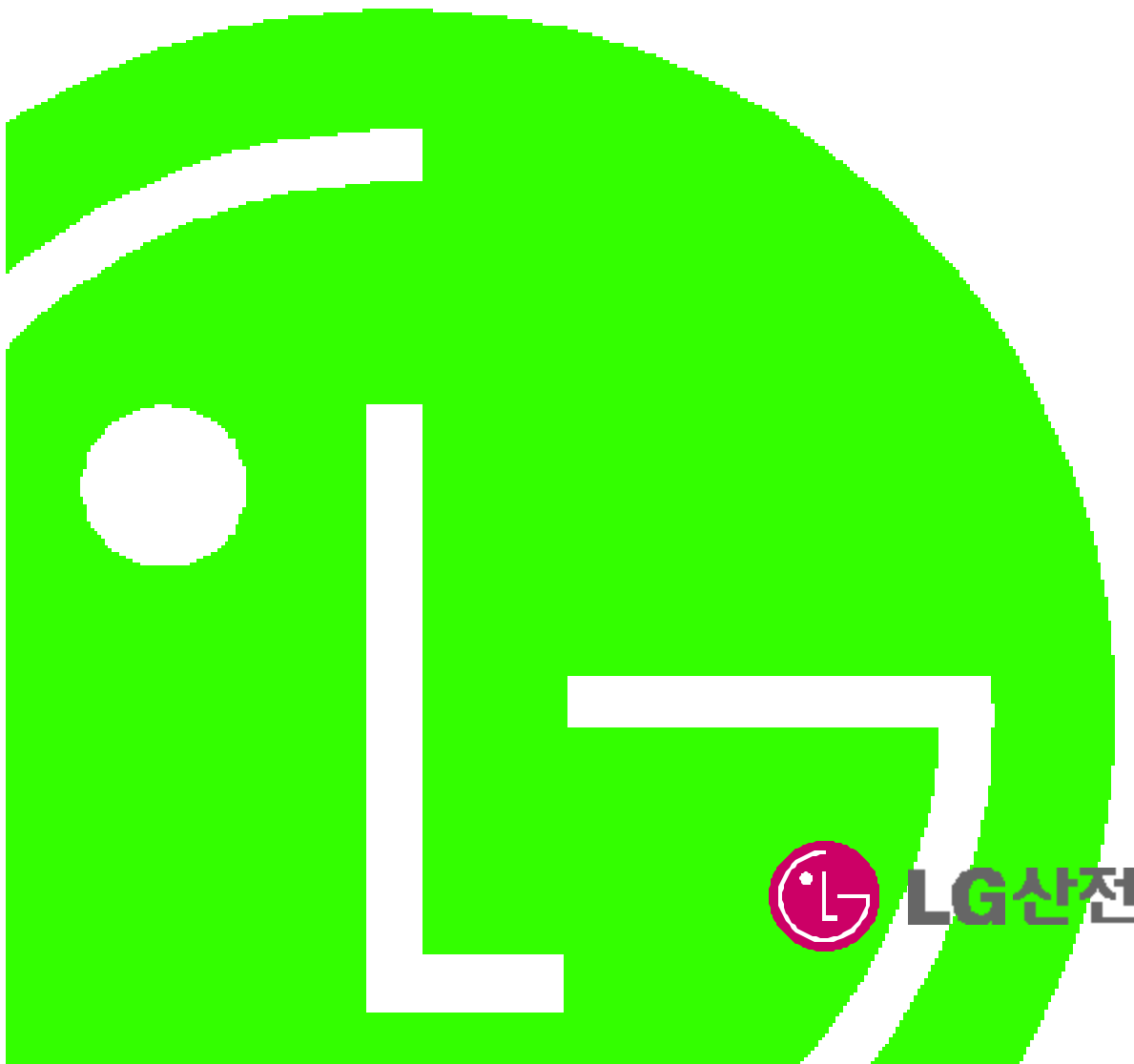
***GLOFA***  
***MASTER-K***

G3L – FUE(O)A/RBE(O)A

G4L – FUE(O)A/RBEA

G6L – FUEA/RBEA

G7L – FUEA







Fnet

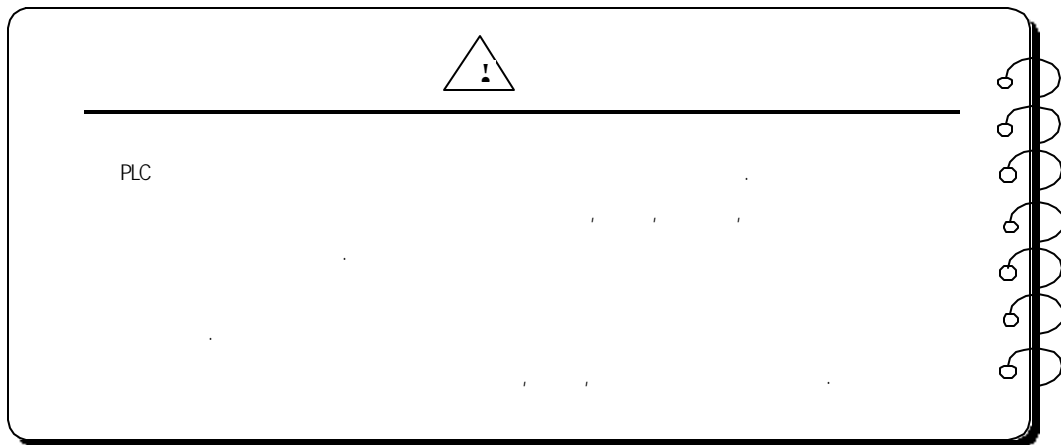
PLC

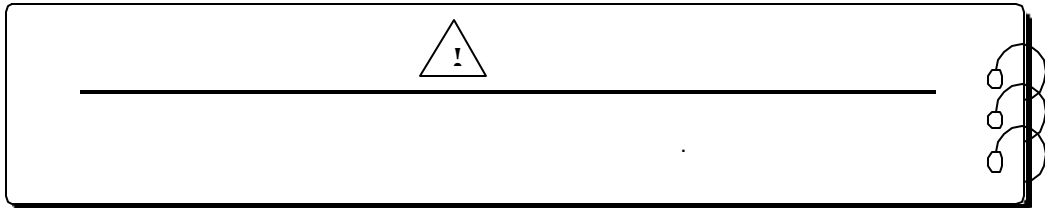
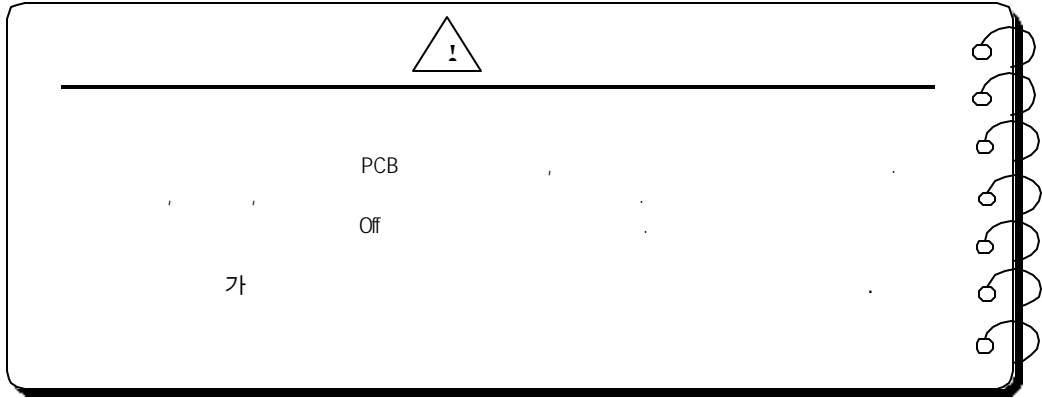
GLOFA/MATER-K CPU



2

가







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1.1

GLOFA, MASTER-K PLC Fnet  
 . Fnet / , ,  
 ,  
 가 ( )  
 ( ) .  
 가 , /  
 Fnet GLOFA MASTER-K ,

- 1) GLOFA-GM MASTER-K Fnet Fnet
- 2) GMWIN V3.0/KGL-WIN V2.0
- 3) , GM7-Fnet GMWIN V3.42/GM7 CPU 0/S V1.4

1.2 Fnet -

Fnet V2.0 GLOFA Fnet MASTER-K Fnet , V2.0

[ 1.2] Fnet V2.0

	Fnet V2.0		Fnet V2.0	
	GLOFA	MASTER-K		
(FMM)	G3L-FUEA	K7F-FUEA	G3L-FUEA	GM3/K1000S Fnet( )
	G3L-FUOA	K7F-FUOA	G3L-FUOA	GM3/K1000S Fnet( )
	G4L-FUEA	K4F-FUEA	G4L-FUEA	GM4/K300S Fnet( )
	G4L-FUOA	-	G4L-FUOA	GM4/K300S Fnet( )
	G6L-FUEA	K3F-FUEA	G6L-FUEA	GM6/K200S Fnet( )
	G7L-FUEA	-	G7L-FUEA	GM7 Fnet( )
(FSM)	G3L-RBEA	K7F-RBEA	G3L-RBEA	GM3/K1000S Fnet( )
	G3L-RBOA	K7F-RBOA	G3L-RBOA	GM3/K1000S Fnet( )
	G4L-RBEA	K4F-RBEA	G4L-RBEA	GM4/K300S Fnet( )
	G6L-RBEA	K3F-RBEA	G6L-RBEA	GM6/K200S Fnet( )
	GOL-FUEA		Fnet	
	GOL-FREA		( )	
	GOL-FOEA		/	
	GOL-SMQA		16	
	GOL-SMHA		DC24V 8 / 8	
	GOL-SMIA		DC24V 16	
	GOL-FAPA / GOL-FACA / GOL-FABA			

1.3 Fnet

Fnet [ 1.3]

[ 1.3] Fnet

Fnet	(FMM)	( )	I/O	G0L -FUEA		
				G3L -FUEA	GM1 , GM2 , GM3 /K1000S	
				G4L -FUEA	GM4 /K300S	
				G6L -FUEA	GM6 /K200S	
				G7L -FUEA	GM7 /K80S	
				G3L -FUOA	GM1 , GM2 , GM3 /K1000S	
	(FSM)	( )		G4L -FUOA	GM4 /K300S	
				G3L -RBEA	GM3 /K1000S	
				G4L -RBEA	GM4 /K300S	
				G6L -RBEA	GM4 /K300S	
				G0L -SMQA		
				G0L -SMIA		
	(FOM)	/		/	G0L -SMHA	
					G3L -RBOA	GM3 /K1000S
					G0L -FREA	
					G0L -FOEA	
G0L -FACA G0L -FAPA G0L -FABA						

2

2.1

(Fnet Master Module:FMM)

I/O Fnet .

(Fnet Slave Module:FSM)

CPU Fnet .

(Fnet Option Module)

, , Fnet .

CPU 가 /  
GMWIN/KGLWIN .

I/O  
PLC PLC CPU , I/O

Fnet , OSI 7 3  
. 3 H2(1Mbps ), H1(31.23Kbbs ), (Wireless)  
, Scheduled Circulated Token bus ,  
가 .

(Token)  
Physical Medium .

Fnet  
Fnet (G3L-FUEA... ). Fnet

(Active Coupler)

가

(Repeater)

E.O.C( / )

가

Manchester Biphase-L

Fnet

, Manchester

Manchester-I Code

(Decode)

(Encode)

CRC(Cyclic Redundancy Check)

가

Physical Layer

110 ,1/2 W

, Fnet

(HS Link)

Fnet

가

, GMWIN/KGL-WIN

GMWIN(GLOFA PLC Programming And Debugging Tool)

GLOFA PLC CPU

가

KGL-WIN(MASTER-K PLC Programming And Debugging Tool)

MASTER-K PLC CPU

가

FAM (FA Manager)

MMI (Man Machine Interface) ,

(Segment)

(Gateway, EOC, )

(Token)

(Network)

(Token)

## 2.2 Fnet

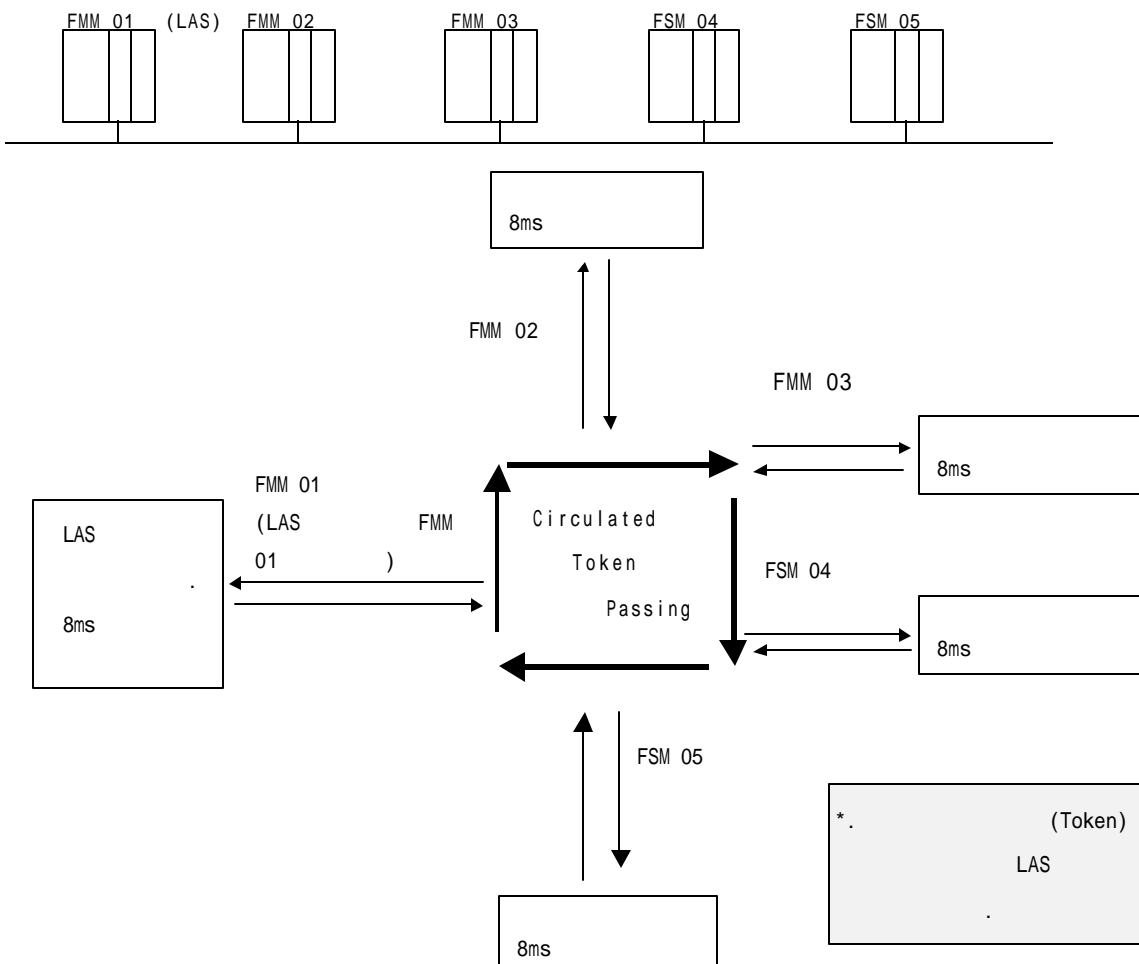
Fnet                      LAS(Link Active Scheduler)                      (Token, )  
 . LAS 가                      FMM                      , FSM                      LAS 가

### 2.2.1 LAS

LAS FMM

- 1) FMM LAS
- 2) LAS
- 3) LAS FMM 가
- 4) LAS

### 2.2.2. (Token) (FMM\_01 LAS 가 )





3

3.1

Fnet

[ 3.1]

No						
1		0	+55			
2		-25	+70			
3		5	95%RH,			
4		5	95%RH,			
5			가		X,Y,Z 10 IEC 61131-2 [ 1]	
		10	f < 57 Hz	-		0.075mm
		57	f 150 Hz	9.8 m/s(1G)		-
				가		
		10	f < 57 Hz	-		0.035mm
		57	f 150 Hz	4.9 m/s(0.5G)		-
6		*	가 : 147 m/s(15G)		IEC 61131-2	
		*	가 : 11 ms			
		*	: (X,Y,Z 3 3 )			
7			± 1,500V		LG	
			: 4kV( )		IEC 61131-2,	
			27 ~ 500 MHz, 10V/m		IEC 61131-2,	
		/	(24V ) 2kV 1kV	(24V ) 0.25kV	IEC 61131-2, IEC 1000-4-4	
8		가 , 가				
9		2000m				
10	[ 2]	2				
11						

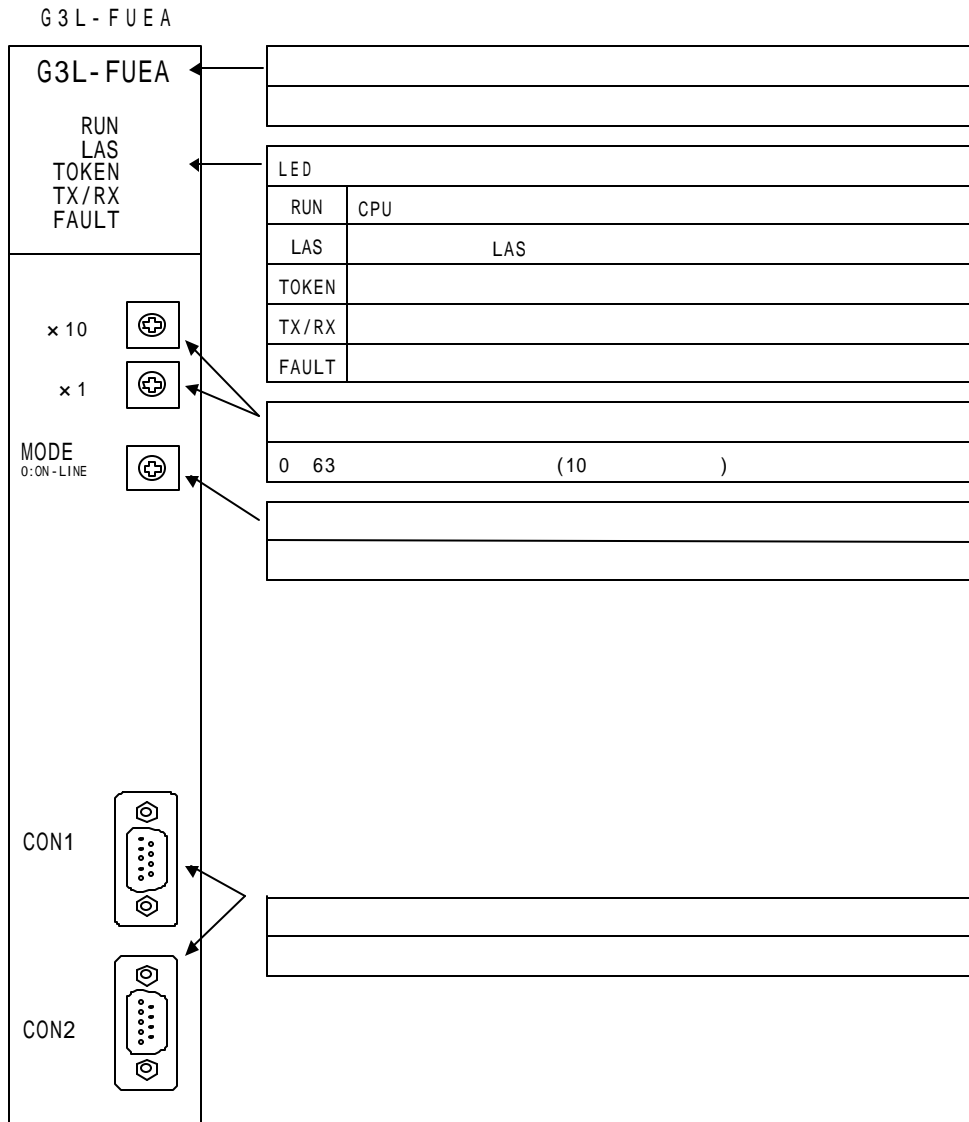
[ 1] IEC(International Electrotechnical Commission : )  
:  
[ 2] :  
2 ,

3.2

Fnet

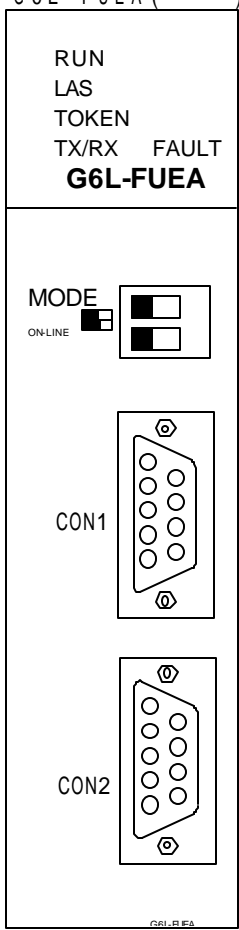
3.2.1 : G3L-FUEA/FU0A, G4L-FUEA/FU0A, G6L-FUEA

1) G3L-FUEA, G3L-FU0A, G4L-FUEA



1) G3L-FU0A  
 2) 3.2.6 Fnet

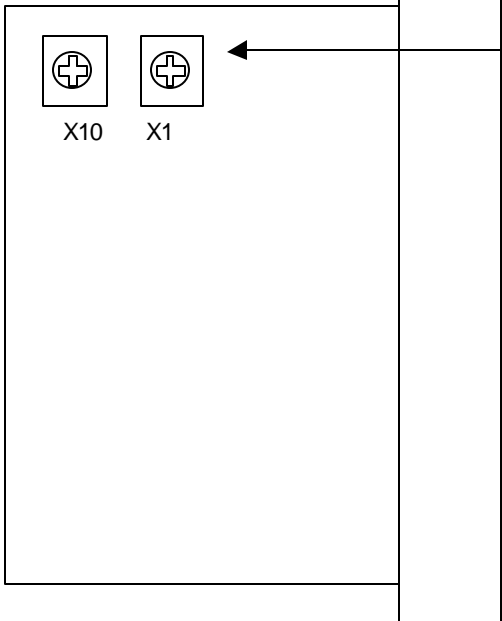
2) G6L-FUEA ( )



LED	
RUN	CPU
LAS	LAS
TOKEN	
TX/RX	
FAULT	

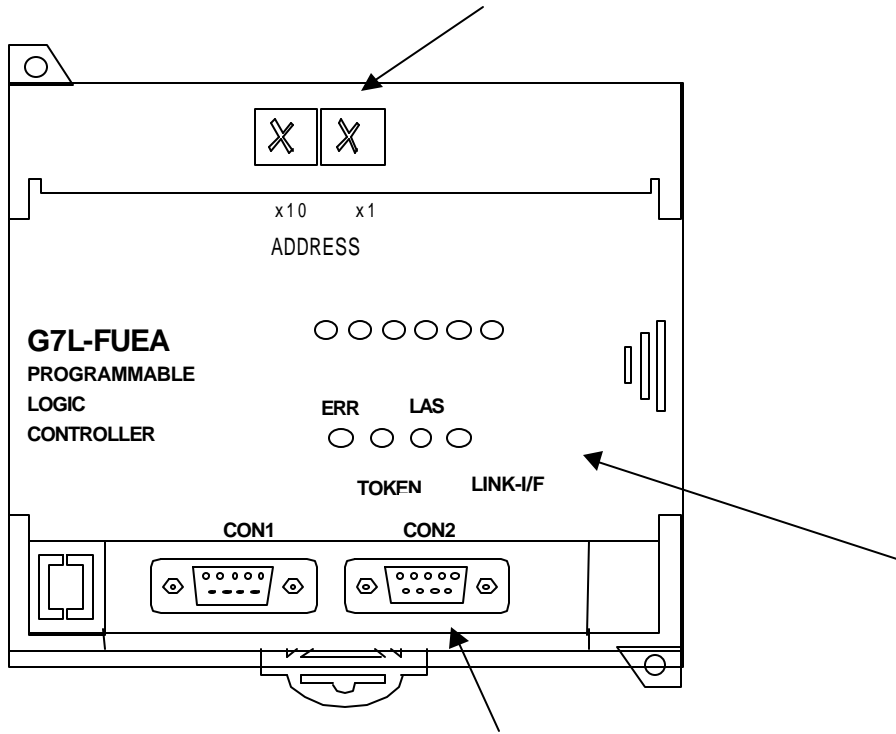



G6L-FUEA ( )



0 ~ 63 (10 )

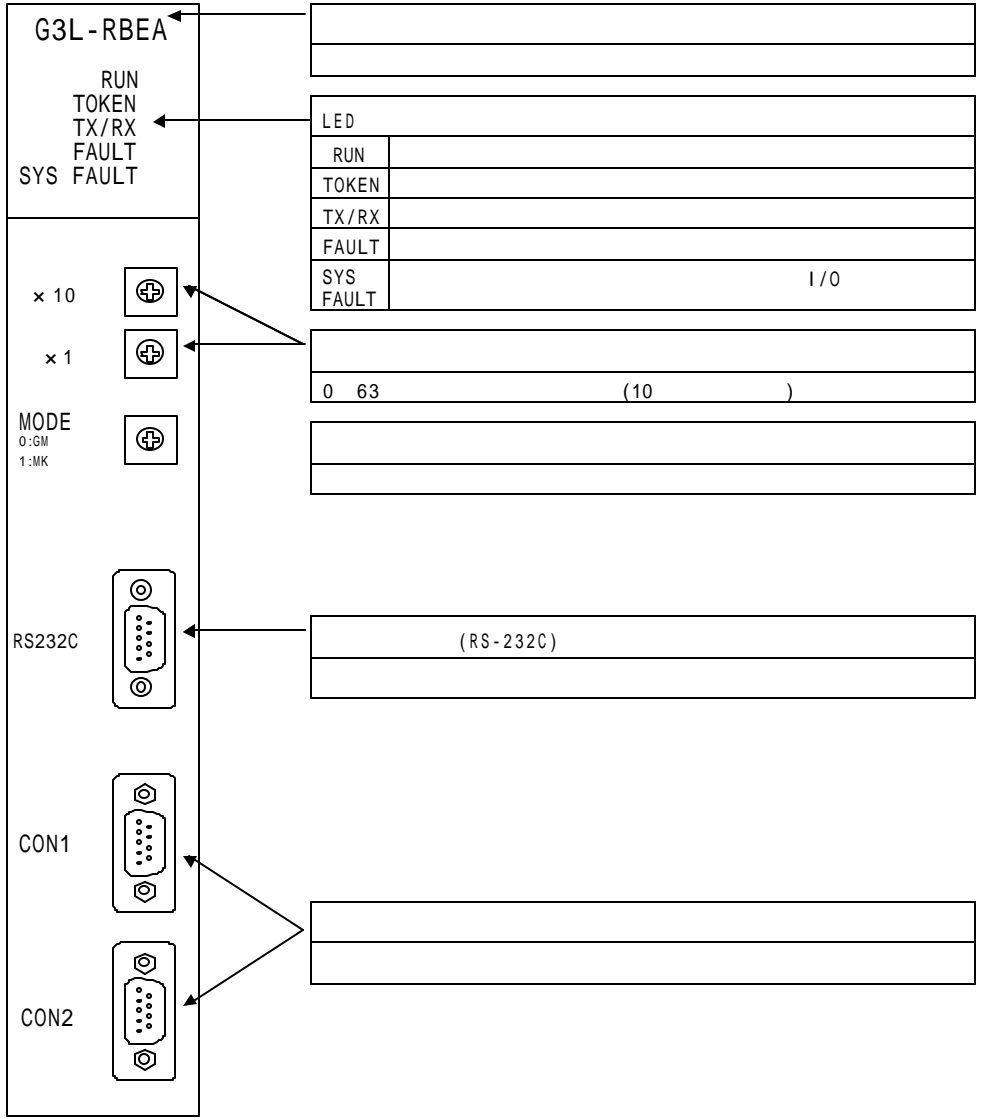
3) G7L-FUEA



LED	ERR : ( : ) TOKEN : LAS : LAS ( ) LINK-I/F : /
( )	(0 ~ 63) 10 X10 : 10 (0 ~ 6) X1 : 1 (0 ~ 9)
	CON1/2 : (9 )

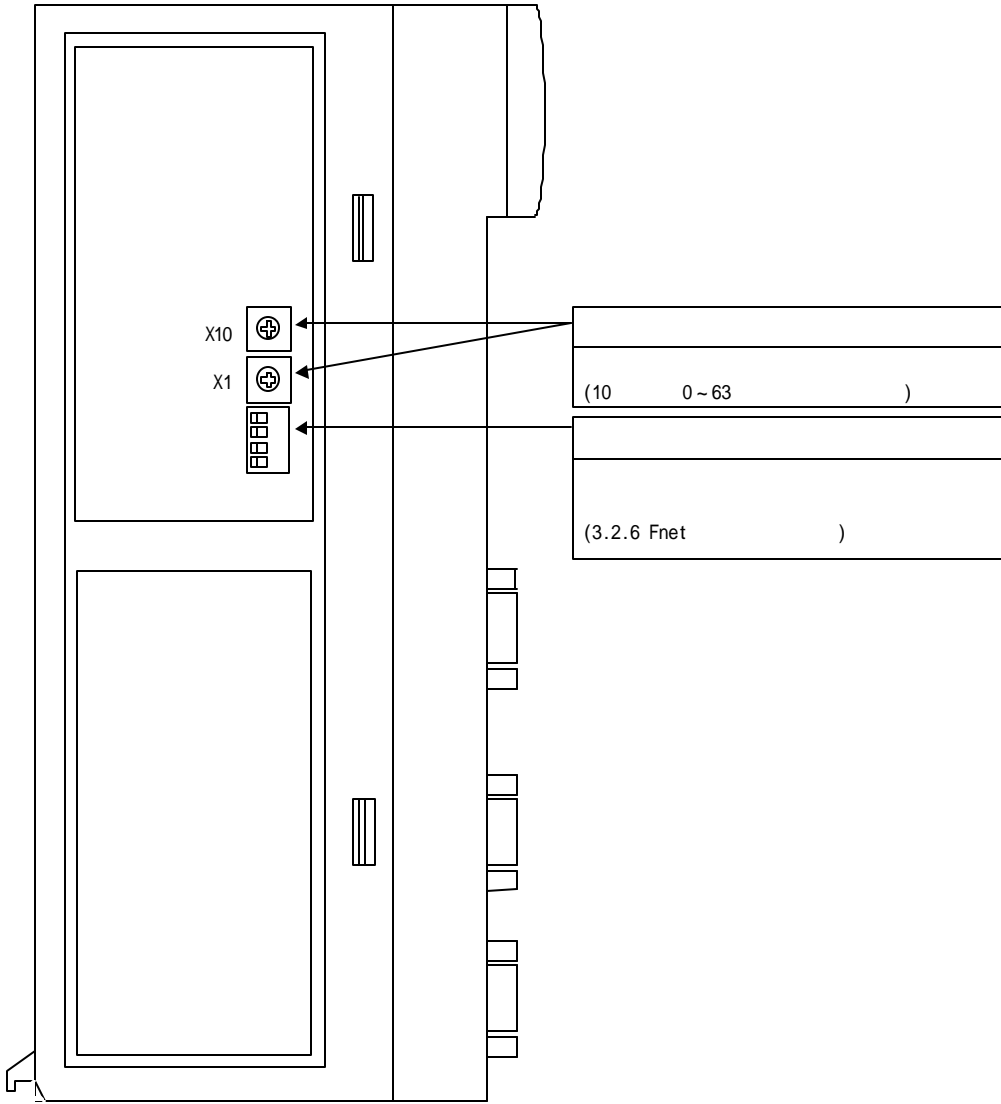
3.2.2 : G3L-RBEA, G3L-RBOA, G4L-RBEA, G6L-RBEA

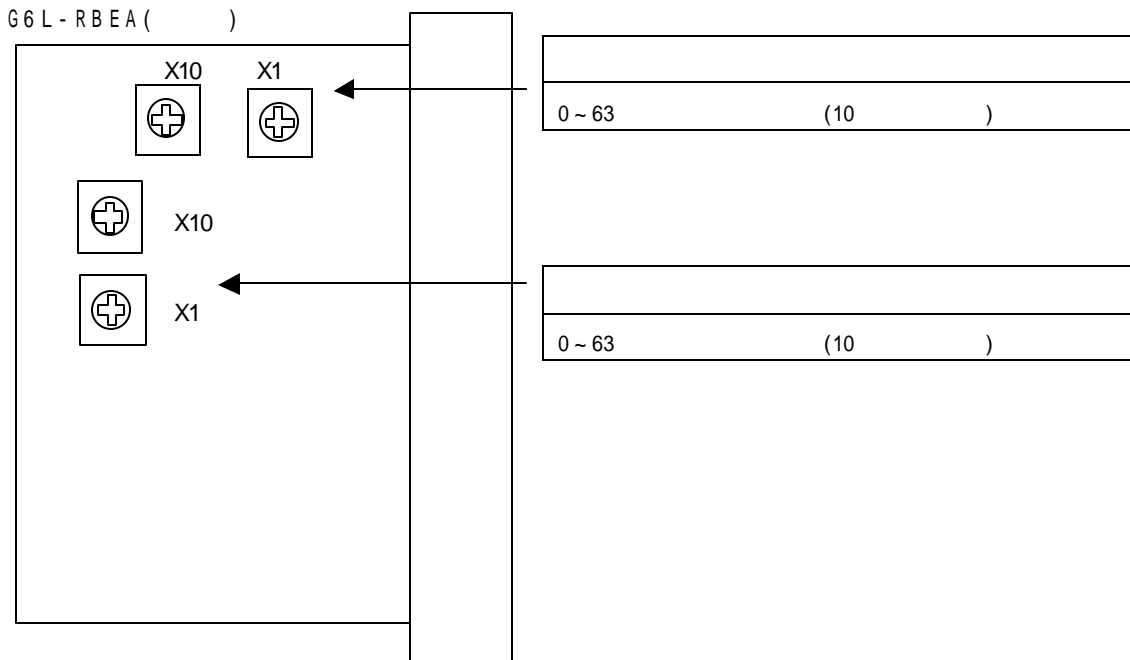
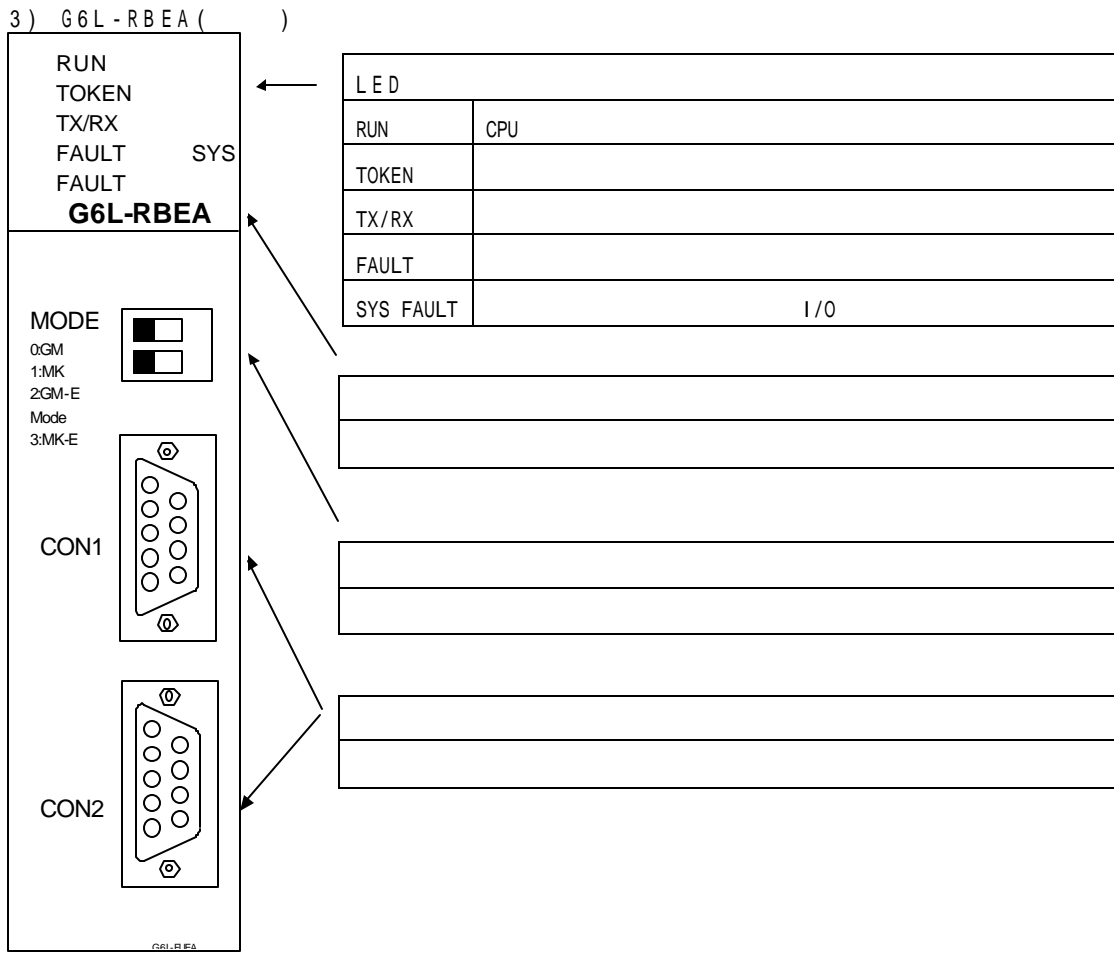
1) ( G3L-RBEA )



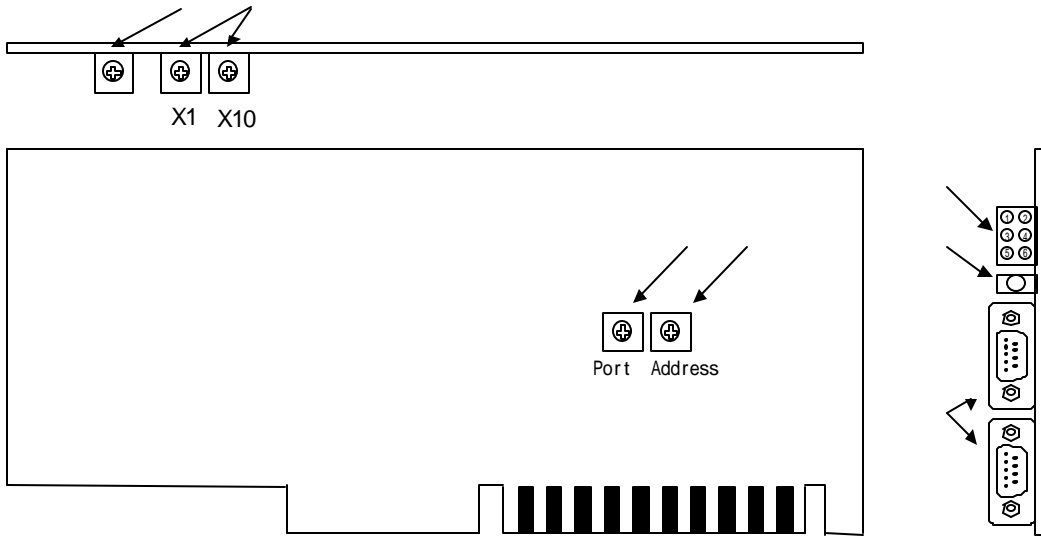
1) G3L-RBOA , G4L-RBEA RS-232C 가

2) ( G3L - RBEA )





3.2.3 GOL-FUEA ( ISA BUS )



0	3E0	FC00
1	3C0	F800
2	3A0	F400
3	380	F000
4	360	EC00
5	340	E800
6	320	E400
7	300	E000
8	2E0	DC00
9	2C0	D800
A	2A0	D400
B	280	D000
C	260	CC00
D	240	C800
E	220	C400
F	200	C000

LED		
1	POWER	
2	RUN	CPU
3	LAS	LAS
4	TOKEN	
5	TX/RX	
6	FAULT	
0	63	.(10 )
Reset		

1) 3.2.6 Fnet  
 2) 5 (340), 9 (D800)  
 3) ,  
 CONFIG.SYS DEVICE=C:\WINDOWS\EMM386.EXE NOEMS X=D800 -DBFF(  
 9 D800 )



3.2.4 Fnet LED

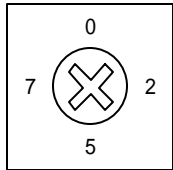
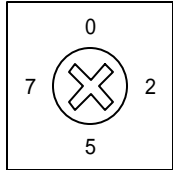
	LED	LED	LED On	LED Off
G3L-FUEA	RUN	CPU		
G3L-FUOA	LAS	LAS		
G4L-FUEA	TOKEN			
G4L-FUOA	TX/RX			
G6L-FUEA				
G7L-FUEA	LINK-I/F			OFF
G0L-FUEA	FAULT			
G3L-RBEA	RUN			
G3L-RBOA	TOKEN			
G4L-RBEA	TX/RX			
G6L-RBEA	FAULT			
G6L-RBEA	SYS FAULT	I/O		
G0L-SMQA	PWR		On	Off
G0L-SMIA	TRX			
G0L-SMHA	ERR			

LED

7.1 LED

3.2.5 Fnet

1)

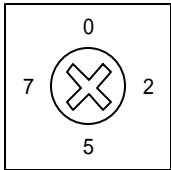
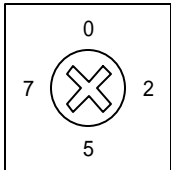
<p>G3L-FUEA/FUOA G3L-RBEA/RBOA G4L-FUEA/FUOA G6L-FUEA G7L-FUEA G4L-RBEA G6L-RBEA G0L-FUEA G0L-SMQA G0L-SMIA G0L-SMHA</p>	<p>× 10</p>  <p>× 1</p> 	<p>(1) 0 63 가 (10 ).</p> <p>(2) .</p> <p>( 0 )</p> <table border="1" data-bbox="873 1619 1242 1759"> <tbody> <tr> <td></td> <td></td> </tr> <tr> <td>× 10</td> <td>10</td> </tr> <tr> <td>× 1</td> <td>1</td> </tr> </tbody> </table> <p>(3) GM6 가 PCB .</p>			× 10	10	× 1	1
× 10	10							
× 1	1							

2)

Fnet

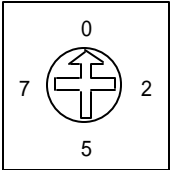
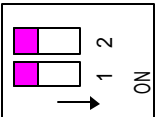
( ) .

Fnet

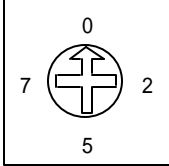
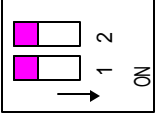
G3L-RBEA G3L-RBOA G4L-RBEA G6L-RBEA GOL-SMQA GOL-SMIA GOL-SMHA	<p>× 10</p>  <p>× 1</p> 	<p>(1) 0 63 가 (10 ) .</p> <p>(2) .</p> <p>( 0 )</p> <table border="1"> <tr> <td></td> <td></td> </tr> <tr> <td>×10</td> <td>10</td> </tr> <tr> <td>× 1</td> <td>1</td> </tr> </table>			×10	10	× 1	1
×10	10							
× 1	1							

3.2.6 Fnet

1)

G3L-FUEA G3L-FU0A GOL-FUEA	<p>MODE 0:ON LINE</p> 	<p>0 . . . . .</p> <table border="1"> <tr> <td></td> <td></td> </tr> <tr> <td>0</td> <td></td> </tr> </table>			0	
0						
G4L-FUEA G6L-FUEA	<p>MODE 0:ON-LINE</p> 	<table border="1"> <tr> <td></td> <td></td> </tr> <tr> <td>0</td> <td></td> </tr> </table>			0	
0						

2) ( GM / MK : GM6 )

G3L-RBEA G3L-RBOA	<p>MODE</p> <p>0: GM 1: MK</p> 	<table border="1"> <tr> <td></td> <td>0, 1</td> </tr> <tr> <td>0</td> <td>GLOFA ( )</td> </tr> <tr> <td>1</td> <td>MASTER-K</td> </tr> </table>		0, 1	0	GLOFA ( )	1	MASTER-K
	0, 1							
0	GLOFA ( )							
1	MASTER-K							
G4L-RBEA	<p>MODE</p> <p>0: GM 1: MK</p> 	<ul style="list-style-type: none"> <li>GLOFA/MASTER-K I/O 가 GLOFA MASTER-K</li> </ul>						

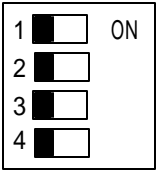






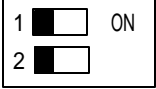






\* 0 GM

3) ( GM6 )

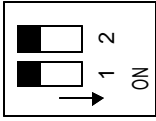
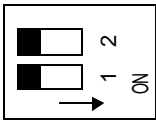
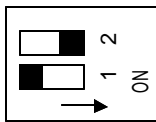
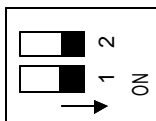
Fnet

I/O

가

G3L-RBEA G3L-RBOA		<table border="1"> <tr> <td></td> <td></td> </tr> <tr> <td></td> <td>가 (Default Reset )</td> </tr> </table>				가 (Default Reset )
						
	가 (Default Reset )					
G4L-RBEA GOL-SMQA GOL-SMHA		<table border="1"> <tr> <td></td> <td></td> </tr> <tr> <td></td> <td>가 (Default Reset )</td> </tr> </table>				가 (Default Reset )
						
	가 (Default Reset )					

4) GM6 ( GM / MK / )

G6L-RBEA	<p>MODE : 0 (GM MODE)</p> 	GLOFA 가
	<p>MODE : 1 (MK MODE)</p> 	MASTER-K 가
	<p>MODE : 2 (GM-E MODE)</p> 	GLOFA 가 ( , GMWIN , OFF 가 0
	<p>MODE : 3 (MK E-MODE)</p> 	MASTER-K 가 ( , KGL-WIN, KLD-150S , 0 OFF 가

1)	Off
2)	GLOFA GMWIN ,
MASTER-K KGL-WIN KLD-150S	.
(6.6.7 )	

4

4.1

4.1.1

: G3L-FUEA/FUOA, G4L-FUEA/FUOA, G6L-FUEA, G7L-FUEA, G0L-

FUEA

[ 4.1.1]

	1Mbps (Fnet )
	Manchester Biphase-L
	( ) 750m
	750m * (6 +1) = 5.25km
	( ) 3km
	3km * (6 +1) = 21km
	(EOC ) + = 64 ( )
	256
	Circulated Token Passing
	Connection Oriented Connectionless
	CRC 16 = $X^{15} + X^{14} + X^{13} + \dots + X^2 + X + 1$

4.1.2

: G3L-RBEA, G3L-RBOA, G4L-RBEA, G6L-RBEA  
 GOL-SMQA, GOL-SMIA, GOL-SMHA

[ 4.1.2]

		1Mbps
		Manchester Biphase-L
	( )	750m
	( )	$750m * (6 + 1)$ = 5,250m
	( )	$3km * (6 EOC+1)$ = 21km
		Link Master Class + Remote Slave Class = 64
		256
		Circulated Token Passing
		Connection Oriented Connectionless

4.1.3

: GOL-FREA, GOL-FOEA, GOL-FACA

1) (GOL-FREA)

[ 4.1.3(A)]

		1Mbps
		Manchester Biphase-L
( )		
		750m
		6
		5.25km( 6 )
		$CRC\ 16 = X^{15} + X^{14} + X^{13} + \dots + X^2 + X + 1$

2) / (GOL-FOEA)  
 [ 4.1.3(B) ] /

	1Mbps
	Manchester Biphase-L
( )	,
	3km( )/750m( )
	Regenerating, Reshaping
	CRC 16 = $X^{15} + X^{14} + X^{13} + \dots + X^2 + X + 1$

3) (GOL-FACA)  
 [ 4.1.3(C) ]

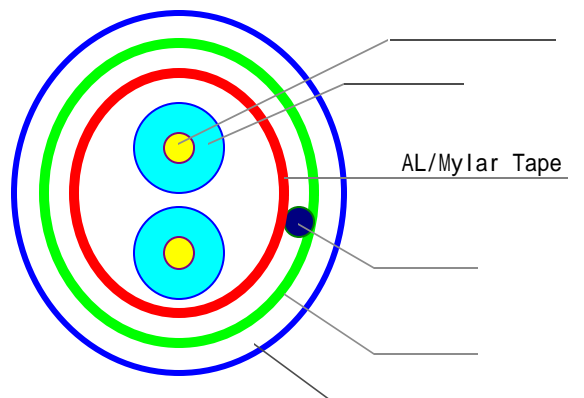
	1Mbps
	Manchester Biphase-L
( )	
	3km
	Regenerating, Reshaping
	CRC 16 = $X^{15} + X^{14} + X^{13} + \dots + X^2 + X + 1$

4.2

4.2.1

: GOC-T□□□ (□□□ , :m)  
 ) 10m : GOC-T010  
 [ 4.2.1] Fnet

Low Capacitance Lan Interface Cable			
LIREV-AMESB			
2*1.0 mm (GS 92-3032,18 AWG)			
LG			
	Ω/km	21.8	
(DC)	V/min	500V 1	
	MEGA Ω-km	1,000	
	pF/m	45	1 kHz
	Ω	120 ± 12	10MHz
	CORE		2
	AWG		18
	NO. /mm		1/1.0
	mm		1.0
	mm		0.9
	mm		2.8





4.2.2

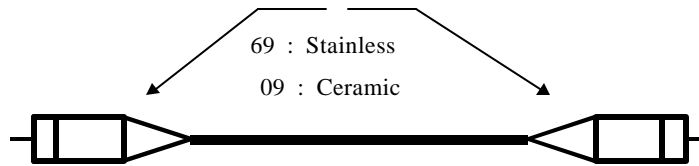
: GOC-F□□□ (□□□ , :m)  
 ) 10m : GOC-F010

[ 4.2.2]

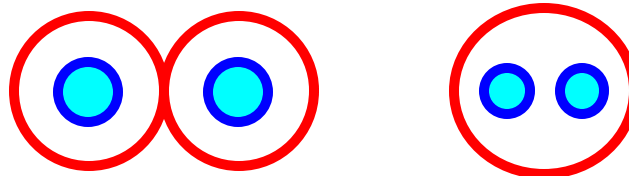
		Y22	:	(for Bi-Directional Communication)
		D22	:	(for Bi-Directional Communication)
		ST - Type		
		(HP)		

		( )	( )
		Y22	D22
(mm)		2.9 * 5.8	4.8
	Loaded(cm)	5.0	7.5
	Unloaded(cm)	3.0	4.8
(kg/m)		16	21

(Core)	62.5	μm
(Cladding)	125	μm
	5	dB/ km
	4.5	dB/ km



) Y226969  
 ST, Stainless



(Y22 ) (D22 )

\* / .

4.3

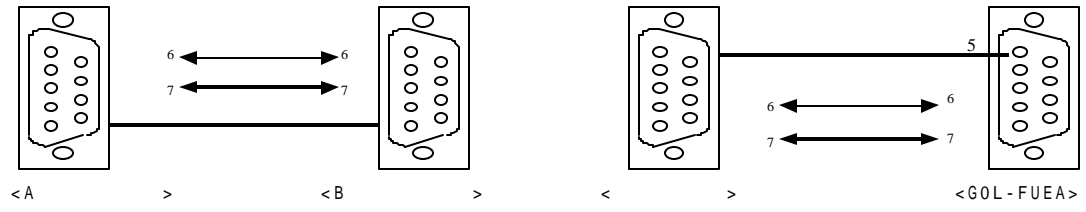
4.3.1 ( )

6, 7, A  
 6 B 6, 7 7 .  
 , 가 .

. GOL-FUEA(PC Fnet )

[ 4.3.1]

GOL-FUEA 5 .



( [ 4.3.1] Fnet ( ) )

4.3.2 ( )

[ 4.3.2(A)]

( )

(GOL-FUEA

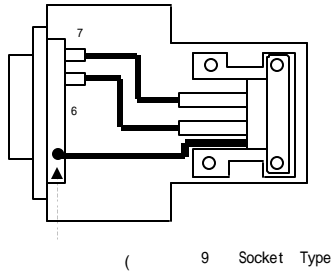
[ 4.3.2(B)]

5

CON1 CON2 5

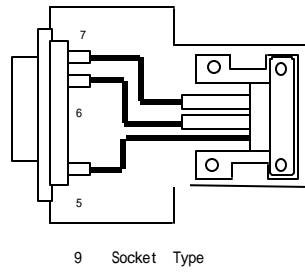
가

).



[ 4.3.2(A)] Fnet

9

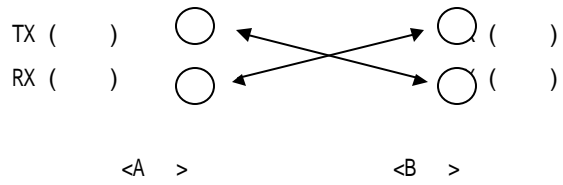


[ 4.3.2(B)] GOL-FUEA

가

4.3.3

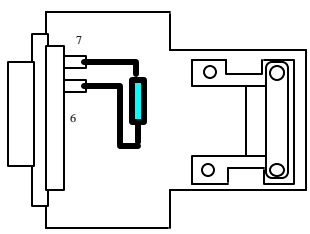
TX( ), A TX( ) -> B RX( ) -> B RX( )



4.4

4.4.1

- : 110 W, 1/2 W



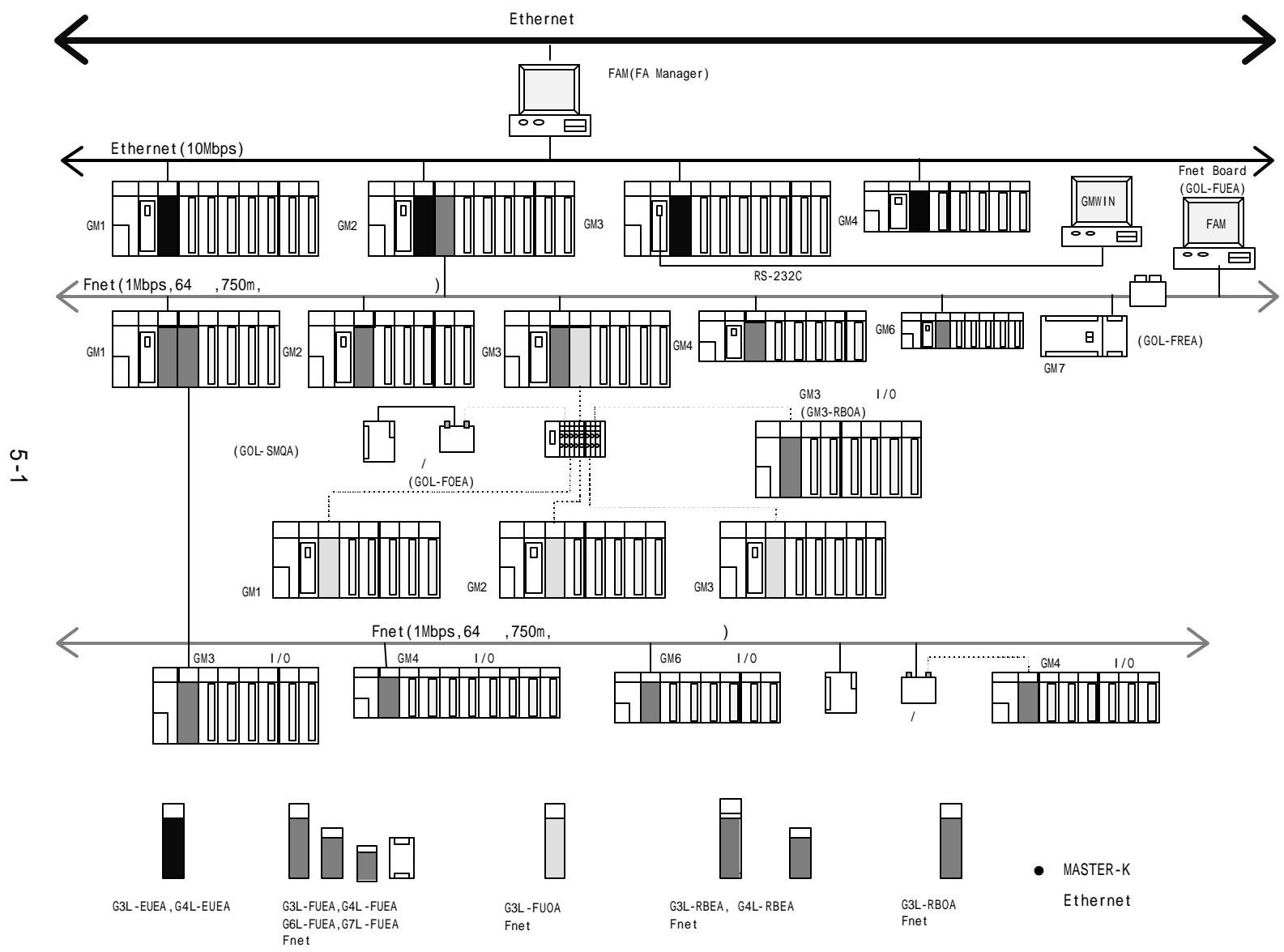
9 Socket Type

(110 , 1/2W)  
( ) .

(GOL-FREA) / (GOL-FOEA)

( 가 )

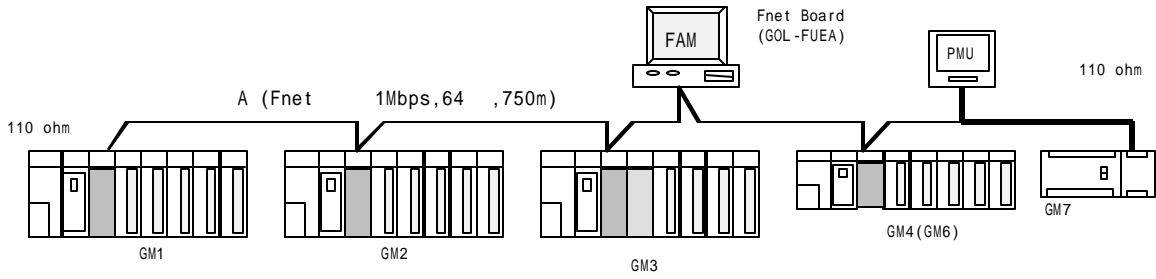
5.1 GLOFA / MASTER - K PLC



5-1

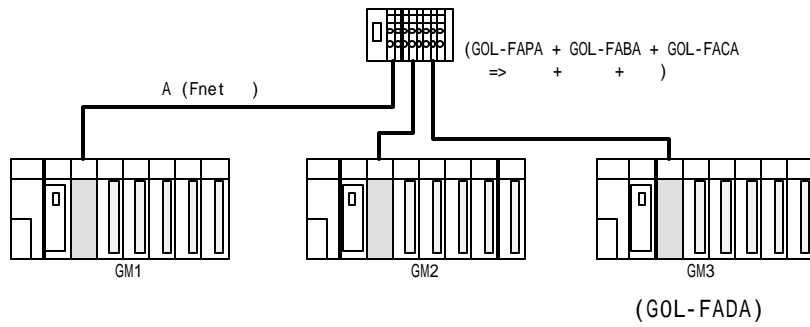
## 5.2 Fnet

### 5.2.1 Fnet ( )

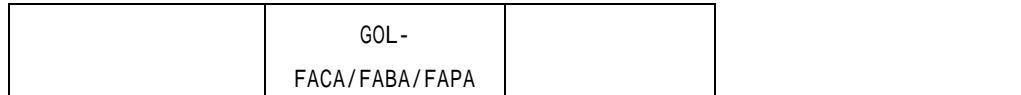


A ( Fnet )		
FAM4.0	GOL - FUEA	0
GM1	G3L - FUEA	1
GM2	G3L - FUEA	2
GM3	G3L - FUEA	3
GM4 (GM6)	G4L - FUEA (G6L - FUEA)	4
GM7	G7L - FUEA	5
PMU - 500	PMO - 500F	6

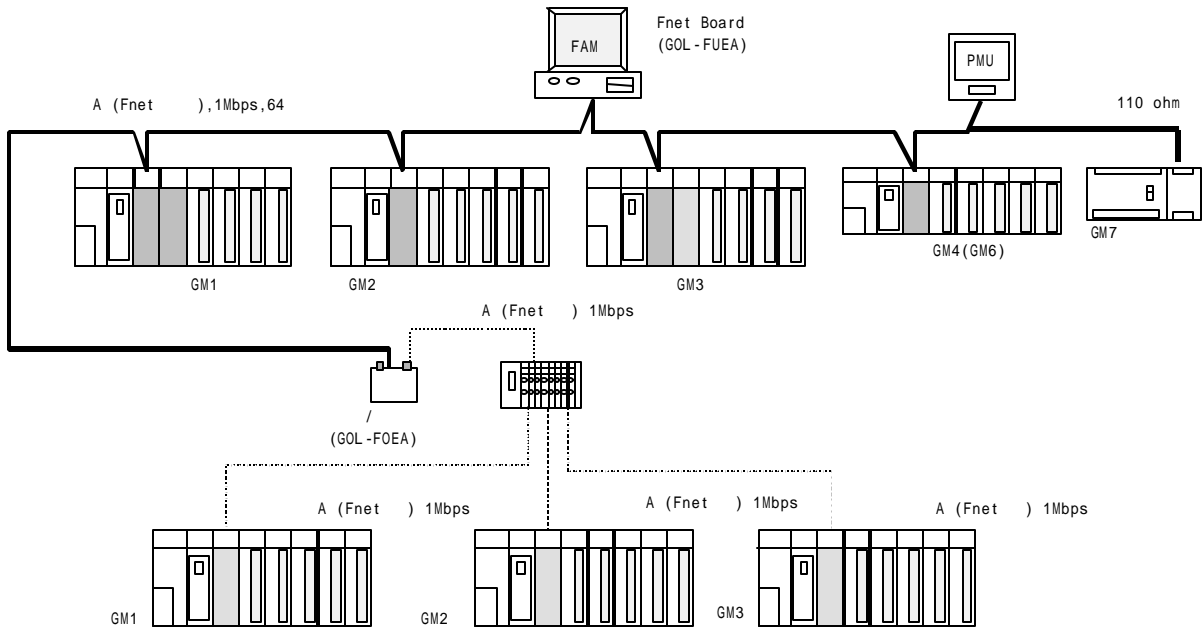
### 5.2.2 Fnet ( )



A ( Fnet )			
GM1	G3L - FUOA	0	→ ( )
GM2	G3L - FUOA	1	→ ( )
GM3	G3L - FUOA	2	



5.2.3 Fnet ( / )



A ( Fnet )					
Fnet			Fnet		
FAM	GOL -FUEA	0	GM1	G3L -FUOA	7
GM1	G3L -FUEA	1 ( 0 )	GM2	G3L -FUOA	8
GM2	G3L -FUEA	2	GM3	G3L -FUOA	9
GM3	G3L -FUEA	3	/	GOL -FOEA	
GM4 (GM6)	G4L -FUEA (G6L -FUEA)	4		GOL -FACA ( )	
GM7	G7L -FUEA	5			
PMU-500	PMU-500F	6			

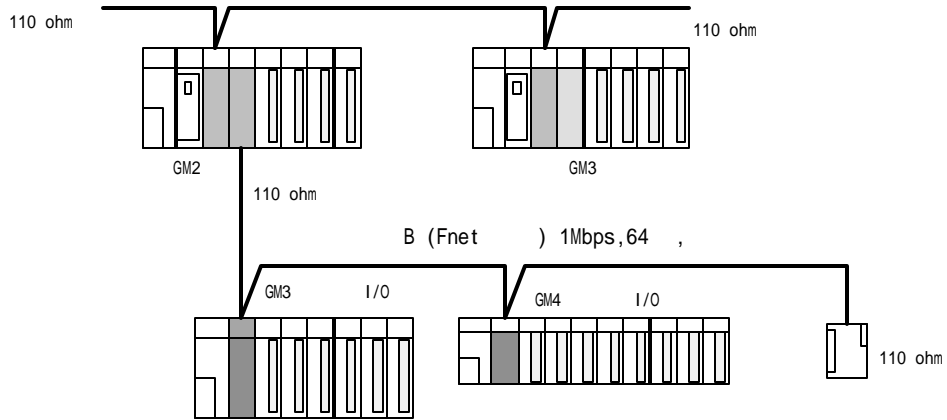
1) /

2) GOL -FAPA( )+GOL -FABA( )+GOL -FACA( )

(GOL-FADA)

5.2.4 Fnet

A (Fnet) 1Mbps,64

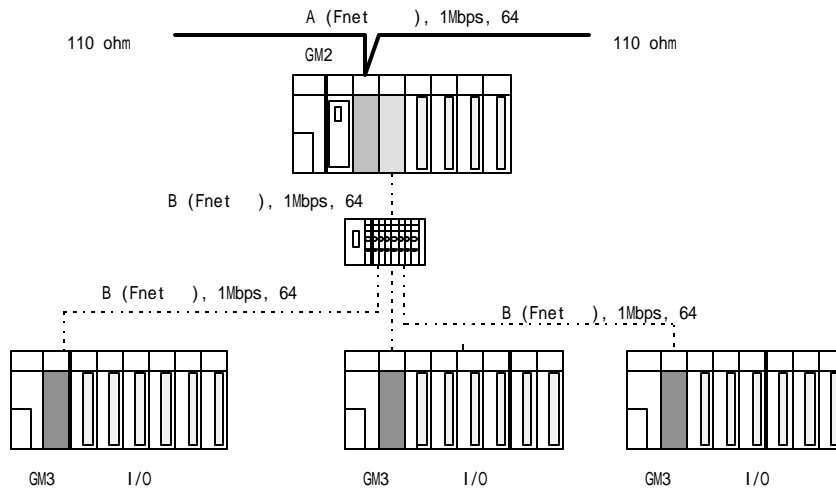


A ( Fnet )		
GM2	G3L -FUEA	0 ( 0 )
GM3	G3L -FUEA	2 ( 0 )

B ( Fnet )		
GM2	G3L -FUEA	1 ( 1 )
GM3 I/O	G3L -RBEA	3
GM4 I/O	G4L -RBEA	4
	GOL -SMQA	5



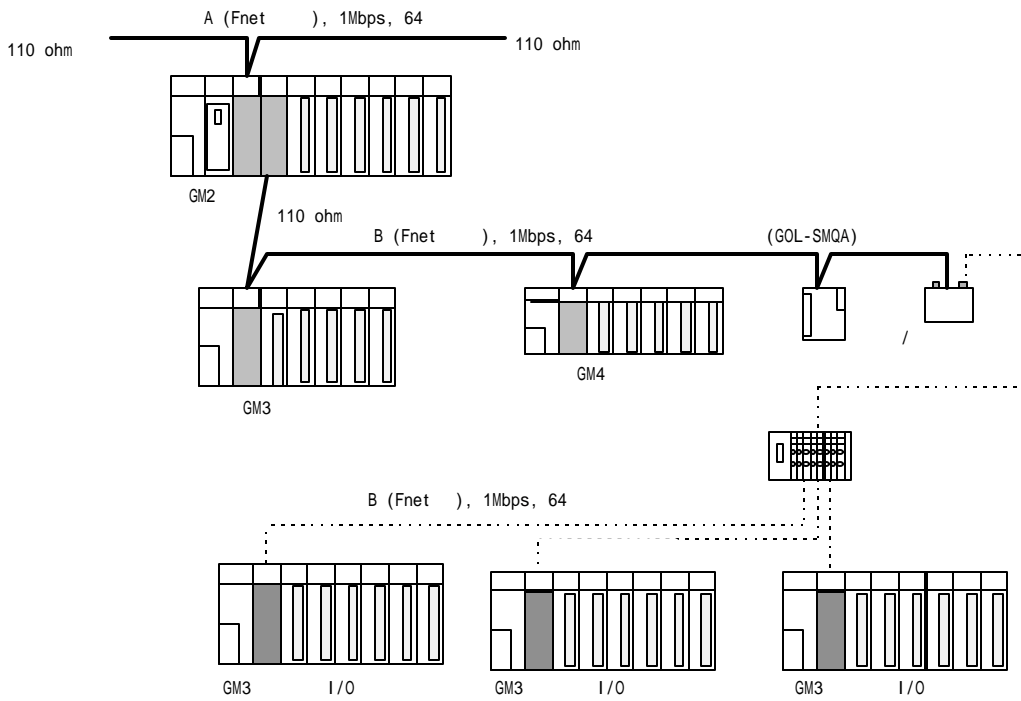
5.2.5 Fnet ( )



A ( Fnet )		
GM2	G3L - FUEA	0 ( 0 )

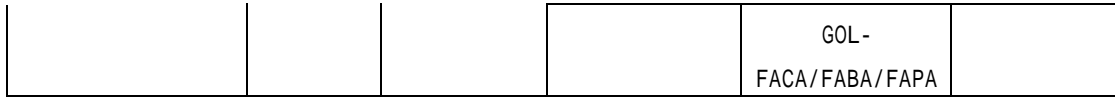
B ( Fnet )		
GM2	G3L - FU0A	1 ( 1 )
GM3 I/O	G3L - RBOA	2
GM3 I/O	G3L - RBOA	3
GM3 I/O	G3L - RBOA	4
	GOL - FACA/FABA/FAPA	

5.2.6 Fnet ( / )

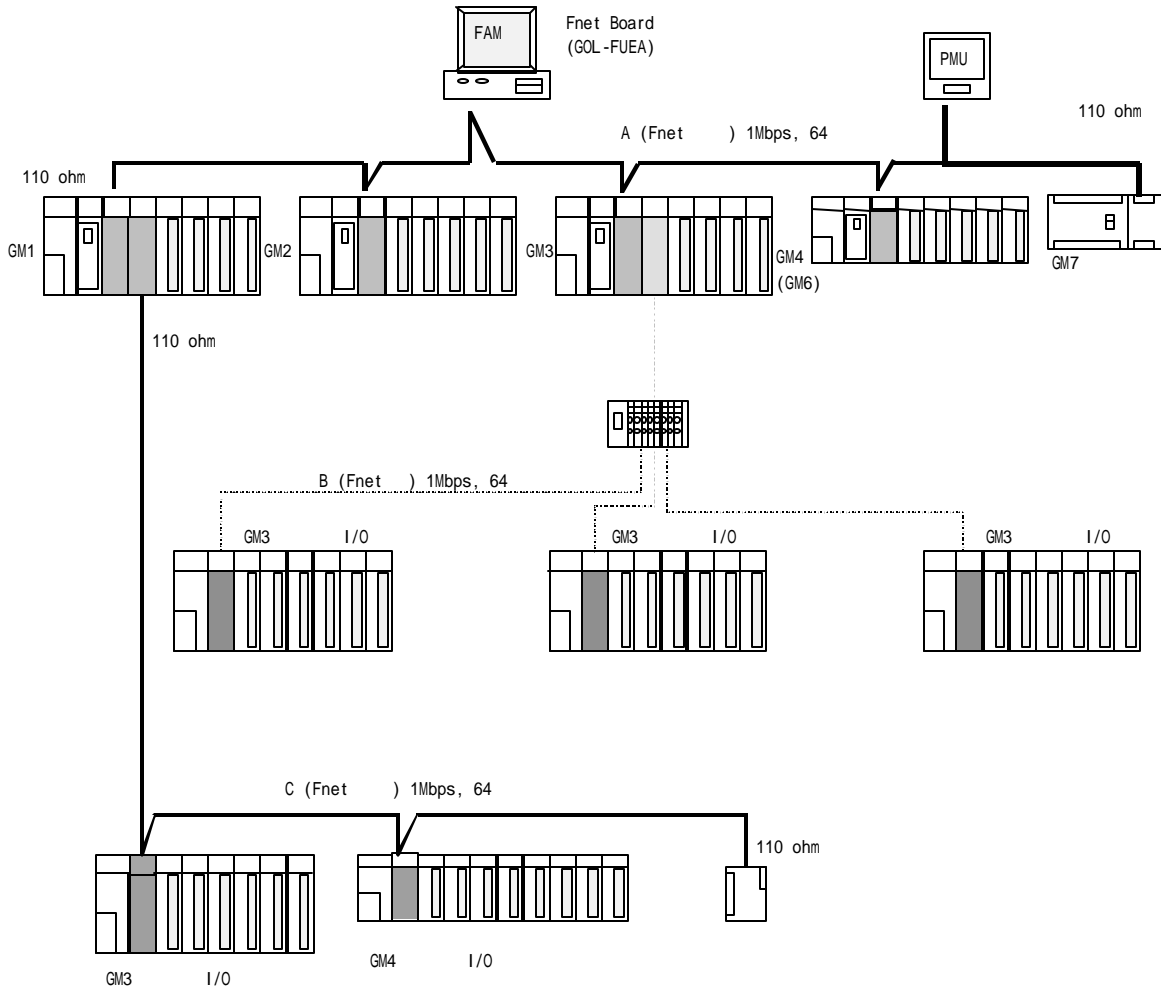


A ( Fnet )		
GM2	G3L - FUEA	0 ( 0 )

B ( Fnet )					
Fnet			Fnet		
GM2	G3L - FUEA	1 ( 1 )	GM3 I/O	G3L - RBOA	5
GM3 I/O	G3L - RBEA	2	GM3 I/O	G3L - RBOA	6
GM4 I/O	G4L - RBEA	3	GM3 I/O	G3L - RBOA	7
	GOL - SMQA	4	/	GOL - FOEA	



5.2.7 Fnet ( / )



A ( Fnet )		
FAM	GOL - FUEA	0
GM1	G3L - FUEA	1 ( 0 )
GM2	G3L - FUEA	3
GM3	G3L - FUEA	4
GM4 (GM6)	G4L - FUEA (G6L - FUEA)	6

GM7	G7L - FUEA	7
PMU - 500	PMO - 500F	8

B ( F net )		
GM3	GOL - FUOA	5 ( 1 )
GM3 I / O	G3L - RBOA	12
GM3 I / O	G3L - RBOA	13
GM3 I / O	G3L - RBOA	14
	GOL - FACA / FABA / FAPA	

C ( F net )		
GM1	G3L - FUEA	2 ( 1 )
GM3 I / O	G3L - RBEA	9
GM4 I / O	G4L - RBEA	10
	GOL - SMQA	11

6

6.1

Fnet 가  
( , G7L - FUEA 가 )

( )

GLOFA

GMWIN, MASTER-K KGL-WIN KLD150S

1 (16 ) Fnet 3,840 가 , 20  
ms 10 가 Fnet V2.0 가

(GLOFA) / (MASTER-K)

가 가

GLOFA GMWIN, MASTER-K KGL-WIN KLD150S  
(Enable)

(16 ) GLOFA Bit, Byte, Word  
MASTER-K (Word)

가

/

[ 6.1] /

		/
	1 (16 )	GLOFA: 가 (Bit, Word ) MASTER-K: (Word)
	20ms( ) ~ 10 *( 1)	(Enable)
	PLC	GLOFA: PLC MASTER-K: PLC
CPU	CPU Run/ Stop/ Pause	CPU

\*( 1) Fnet Version V2.0, CPU Version V3.0

가

6.2

6.2.1

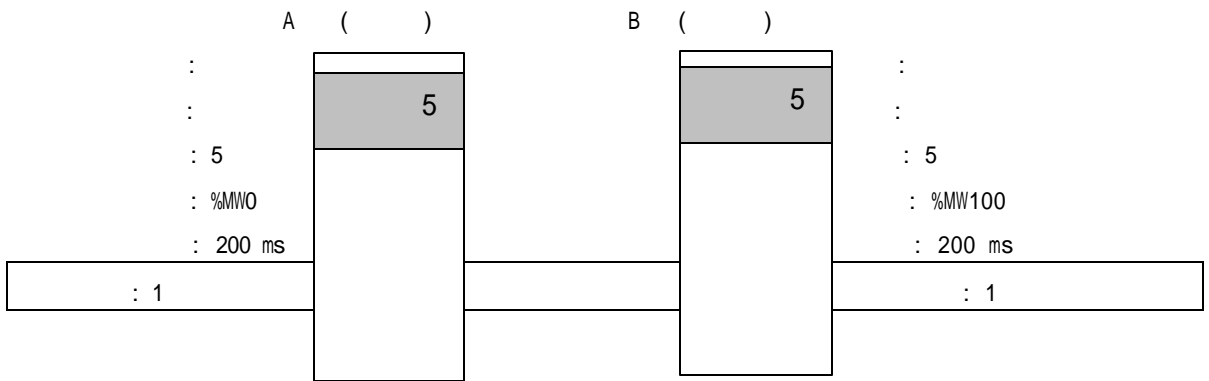
- 가
- 32 64
- 60
- 가 3,840 가
- 가
- 가 20ms ( ) 10
- I/O
- (Keyword)

[ 6.2.1 ]

Fnet	G3L -FUEA/FUOA	3,840	1,920	64 (0-63)	60	
	G3L -RBEA/RBOA	3,840	1,920	64 (0-63)	60	
	G4L -FUEA/FUOA	3,840	1,920	64 (0-63)	60	
	G6L -FUEA	3,840	1,920	64 (0-63)	60	
	G7L -FUEA	3,840	1,920	64 (0-63)	60	
	G4L -RBEA	3,840	1,920	64 (0-63)	60	
	G6L -RBEA	3,840	1,920	64 (0-63)	60	
	G0L -FUEA	3,840	1,920	64 (0-63)	60	

6.2.2

) A %MW0 , B A %MW0 ( B ) .  
 %MW100  
 가 , 0 63 가 32 , 32  
 가 ( ) . A %MW0 (M000  
 ) , 5  
 가 . 5 %MW0 (M000 )  
 A ( B ) , B ,  
 A, 5 , %MW100 (M100 ) .  
 가 ,





6.2.3

1)

HS\_STATE, TRX\_STATE, DEVICE\_MODE, ERROR 가

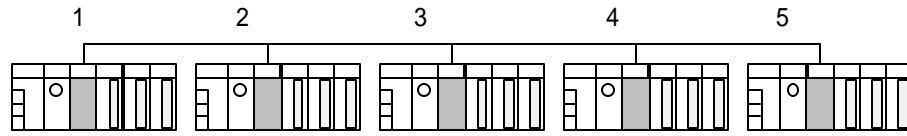
[ 6.2.3]

		LINK_TROUBLE	TRX_MODE	DEV_MODE	DEV_ERROR	HS_STATE
(□= 1,2,3,4 )	_HS□RLINK	_HS□LTRBL	_HS□TRX[n] (n= 0 ~ 63 )	_HS□MOD[n] (n= 0 ~ 63 )	_HS□ERR[n] (n= 0 ~ 63 )	_HS□STATE[n] (n= 0 ~ 63 )
	BIT	BIT	BIT-ARRAY	BIT-ARRAY	BIT-ARRAY	BIT-ARRAY
	가	가	가	가	가	가
	가	가	가	가	가	가

(1) - (\_HS□RLINK)

가 , '0n' , '0n' , '0n' 가 '0ff' '0n' 가

가 가 (RUN) 가



(a)

1	2	3	4	5
:2	:2	:2	:2	:2
:2 (2 )	:2 (1 )	:2 (1 )		
:2 (3 )	:2 (4 )	:2 (5 )		

(b)

[ 6.2.3(A) ] - On

[ 6.2.3(A) ] - 가 'On'

. 5 [ 6.2.3(A) ] (a)

(b)

, 1 - 가 'On'

(1 ) (Link-Enable) 'On' ,

(1 ) RUN ,

(1 ) 가 ,

(1 ) 가 ,

2,3 가 ,

(1 ) (2 ,3 ) 가 RUN ,

가 ,

(1 ) (2,3 ) (4,5 )

가 RUN 가 ,

7 1 - 'On' . PLC 가

- ,

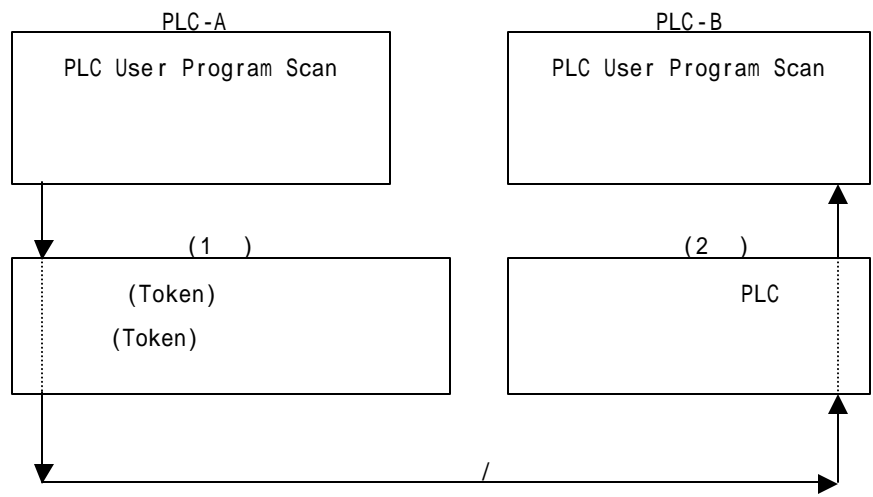
'On' (Link-Enable) 'Off' 'On'

- (2) - (\_HS□LTRBL)  
 - 가 'On' , 'Off' 가 'On' , 'Off' .
- (3) (\_TRX□STATE[0..63])  
 (0~63 )  
 가 'On' , 'Off' .
- (4) (\_HS□MODE[0..63])  
 (0~63 )  
 . RUN 가 'On' ,  
 STOP/PAUSE/DEBUG 'Off' .
- (5) (\_HS□ERR[0..63])  
 (0~63 )  
 PLC 가 'Off' , PLC 가 'On' .
- (6) (\_HS□STATE[0..63])  
 가 , (RUN) , 가 'On' ,  
 'Off' .

(1) ~ (6)  
 □ : (1,2,3,4) .  
 ( 1 1 )  
 [0..63] : [ 6.2.2(E) ] .  
 (0~63 )

6.2.4

1)



[ 6.2.4(A) ]

[ 6.2.4(A) ]

3 가

[ 6.2.4 ]

[ 6.2.8 ]

(Path)	
PLC CPU(A) --> (1 )	PLC-A
(1 ) --> (2 )	+ O/S
(2 ) --> PLC CPU(B)	PLC-B

PLC CPU

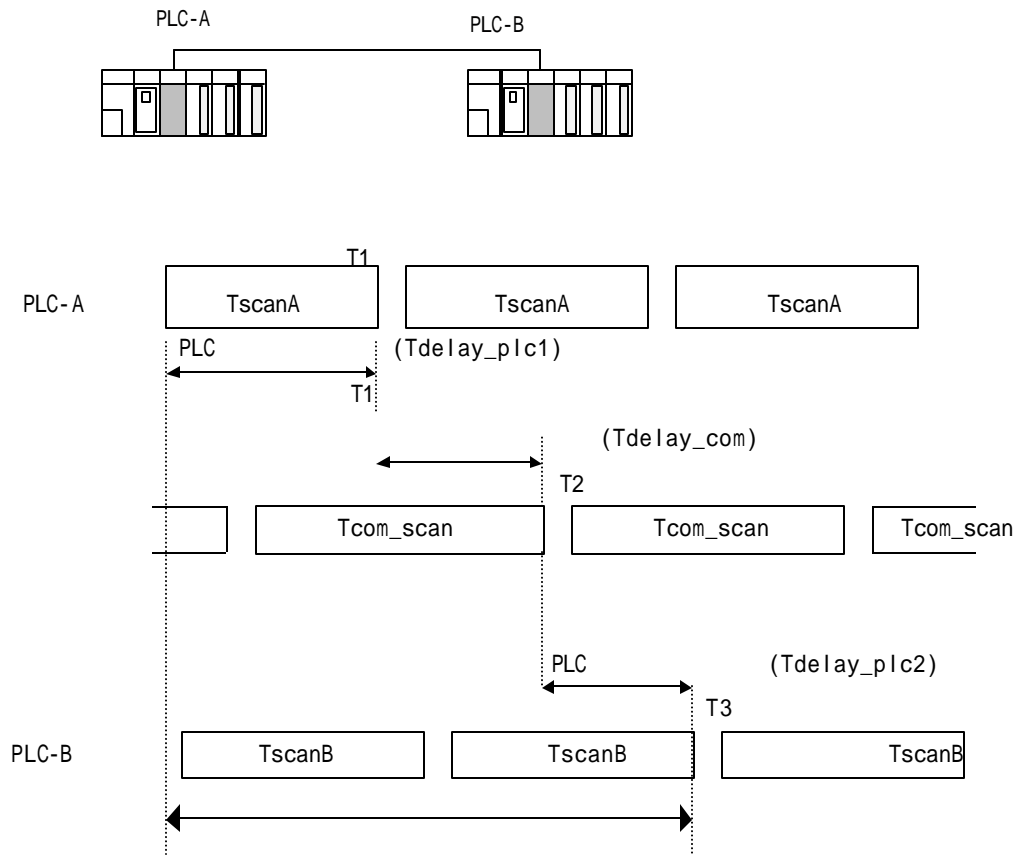
, PLC

가

(Token)

(Token)

[ 6.2.4(B) ] PLC



[ 6.2.4(B) ] PLC

[ 6.2.4(B) ]

$T_1+T_2+T_3$  가

0/S

가



(2)

10 가 512

$$St = Et \times To \times Ntx + Mf \text{ ----- [ 6.2.4(C)]}$$

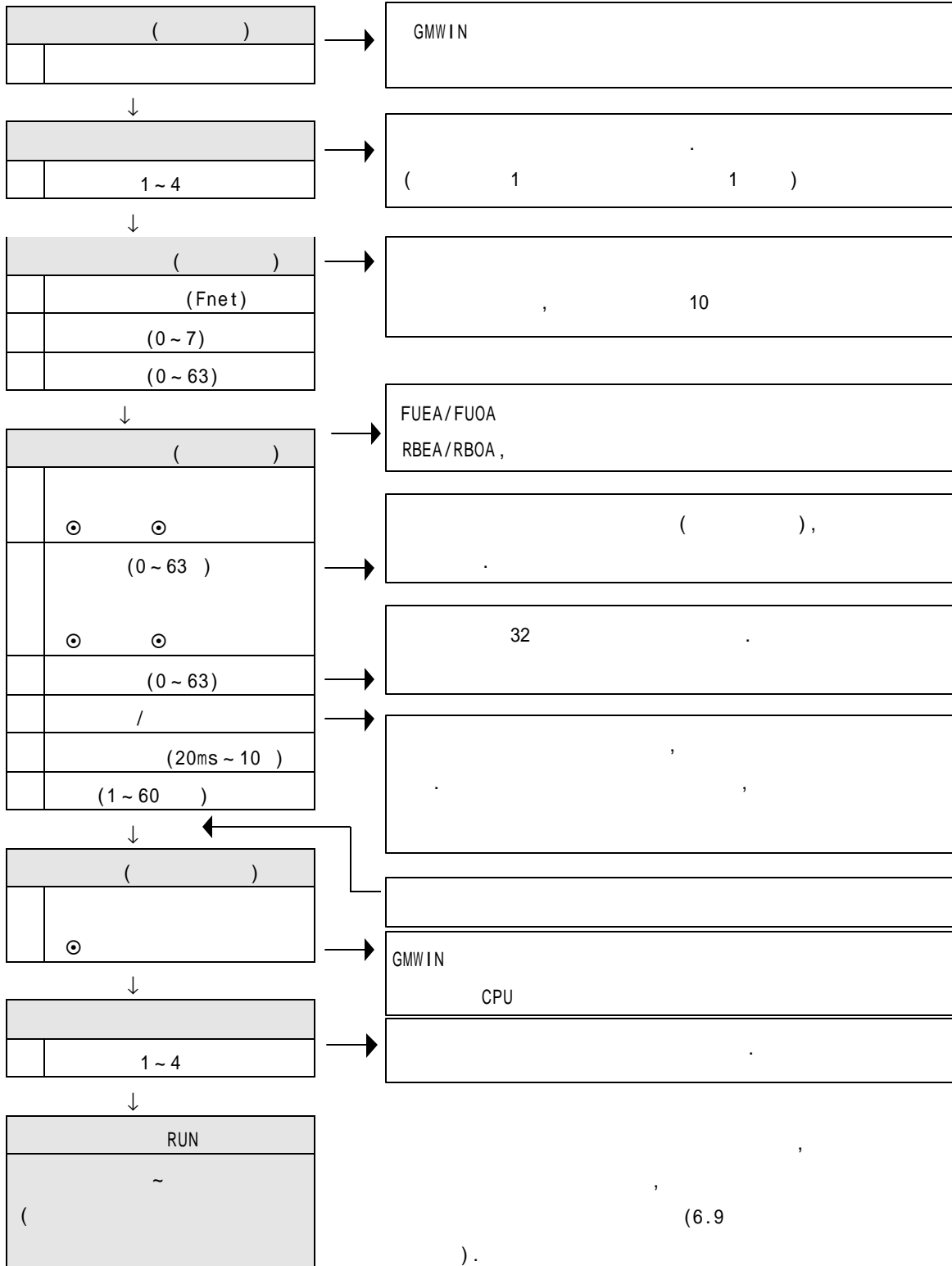
Et = Effective Tx Ratio( )  
 To = Octet time (1 )  
 Ntx = Total Tx number  
 Mf = Margin Factor( )

$$Et = St \times Nf \text{ ----- [ 6.2.4(D)]}$$

St = Total  
 Nf = Factor  
 Fnet 1.5  
 To = Octet Time  
 Fnet : 8 μs  
 Ntx = / ,  
 Fnet : Byte + Variable F/B( ) × 256  
 Mf = O/S  
 Fnet  
 Fnet : 16 ms

6.3 GLOFA

6.3.1





6.3.2

GMWIN

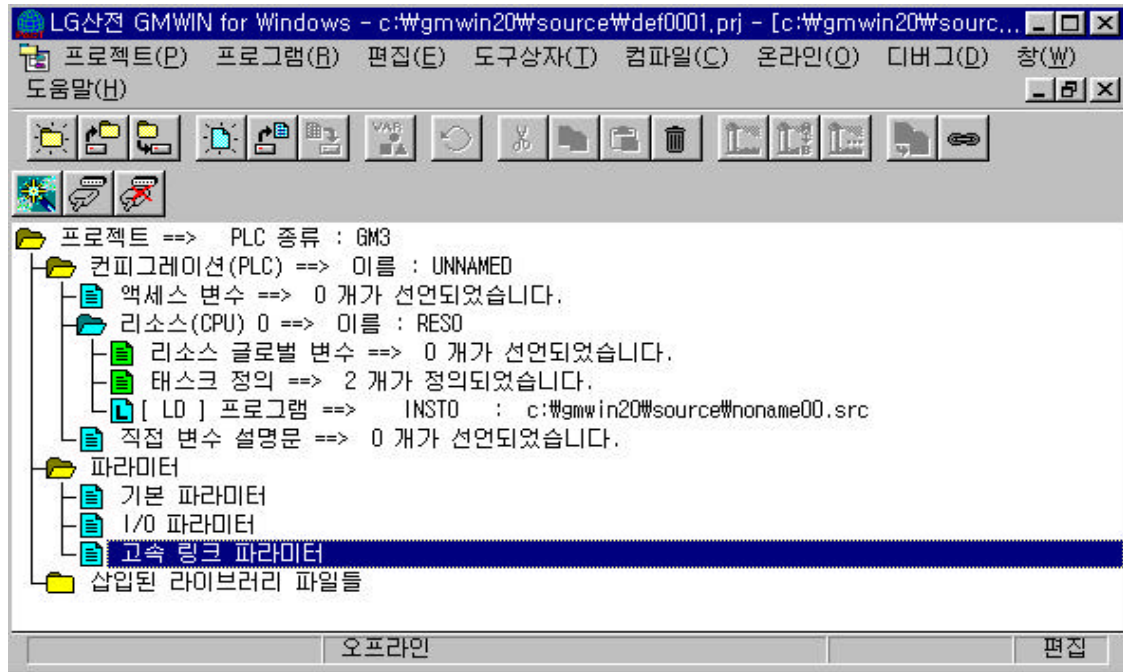
( , G7L-FUEA 가 )

1) GMWIN

[ 6.3.2(A)

[ 6.3.2(B)]

가

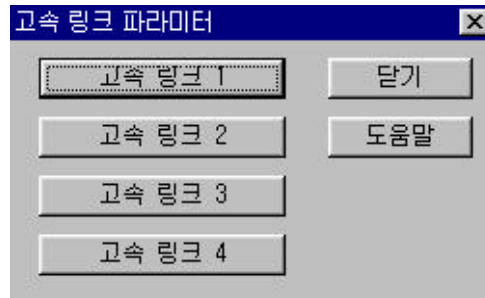


[ 6.3.2(A)] GMWIN

2)

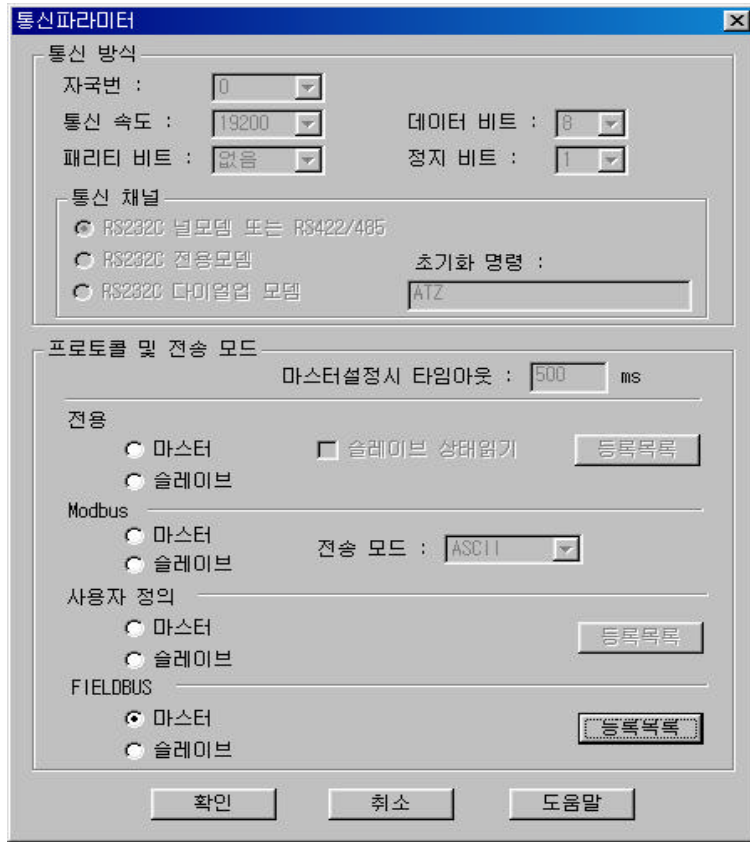
(1)

:



[ 6.3.2(B)]

(2) GM7-Fnet



[ 6.3.2(C)]

(3) : [ 6.3.2(B)] 1 ~ 4 PLC CPU

GLOFA GM1/GM2/GM3 CPU 4 , GLOFA GM4/GM6 2  
 , [ 6.3.2(C)] GM7 1  
 가 .

가)  
 )

1

가 .

[ 6.3.2(A) ] GLOFA CPU 가

[ 6.3.2(A) ] CPU

	가	( 1 )	
GLOFA-GM1	G3L-FUEA, G3L-FU0A	4	가
GLOFA-GM2			
GLOFA-GM3			
GLOFA-GM4	G4L-FUEA, G4L-FU0A	2	
GLOFA-GM6	G6L-FUEA	2	
GLOFA-GM7	G7L-FUEA	1	

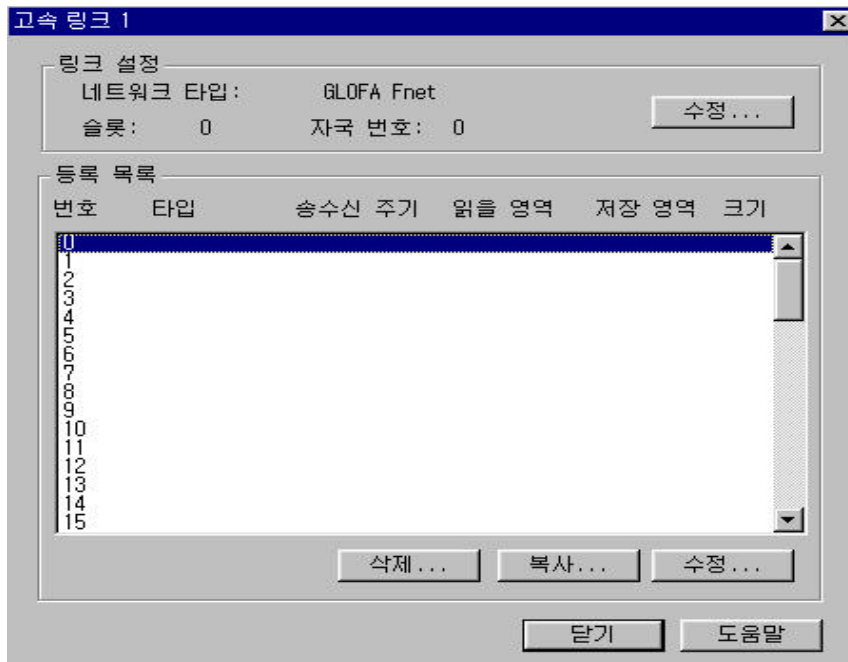
1) (Cnet) ,

3)

[ 6.3.2(B) ]

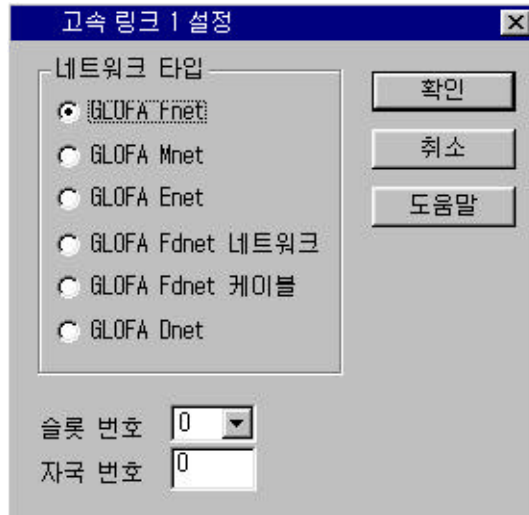
[ 6.3.2(C) ]

가 ,



[ 6.3.2(D) ]

(1)



[ 6.3.2(E) ]

: Fnet .

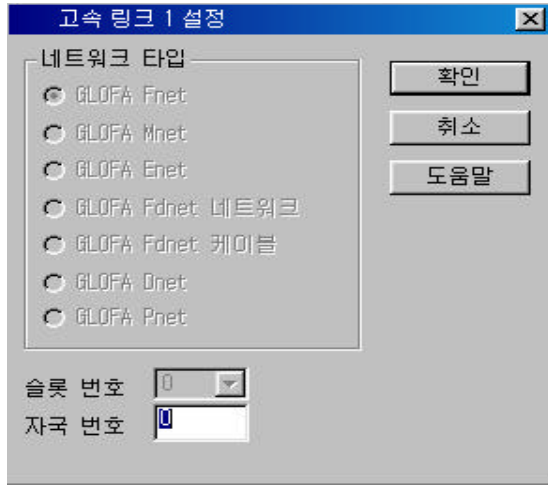
: ' 0 ' ' 7 '

(CPU 0 ).

: . 10 0

63 가 ,

(2) G7L - FUEA



[ 6.3.2(E) ]

: Fnet .

:

: . 10 0

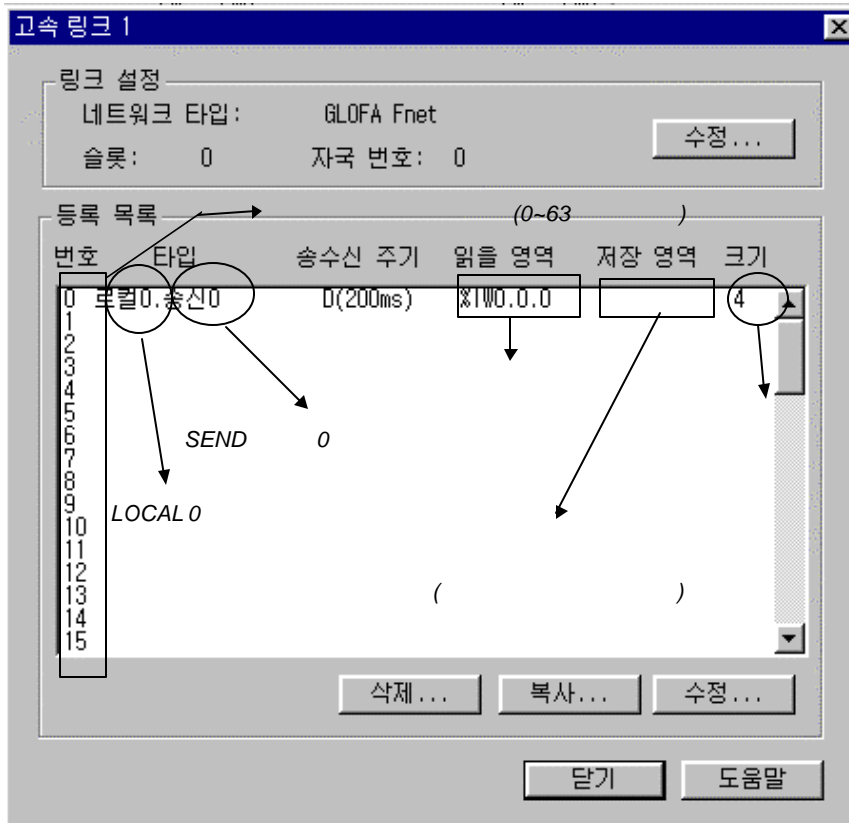
63 가 ,

(3)

‘0’ [ 6.3.2(E) ]



(A)



(B)

- : ' 0 ' ' 63 ' 64

- : \_\_\_\_\_ : G3L-FUEA/FU0A/G4L-FUEA, G6L-FUEA, G7L-FUEA, GOL-FUEA/ ,

\_\_\_\_\_ : G3L-RBEA/RB0A, G4L-RBEA, G6L-RBEA, , .

- : , , 가

\*

[ 6.3.2(B) ]

			0 ~ 63
			( 10 )

- : 가 32 가 , 32

- : 가 32 가 . Fnet 64 가 64 32

:  
 ) , %IW , %QW      %IW      %QW      %MW      100  
 ( : 100      %MW      100  
 ( :  
 16      %IW 0.1.0) .  
 :      %MW , %IW , %QW  
 :      %MW , %IW ,  
 %QW  
 :      (      %MW , %IW , %QW  
 )      (      %QW  
 가 .      가  
 )  
 :      (      %IW  
 가 .      )  
 %MW , %IW , %QW      . CPU  
 가      [ 6.3.4(C)]

[ 6.3.2(C)]

								CPU
		%IW	%QW	%MW	%IW	%QW	%MW	
					X	X	X	CPU
		X	X	X				
						X	X	
		X		X				

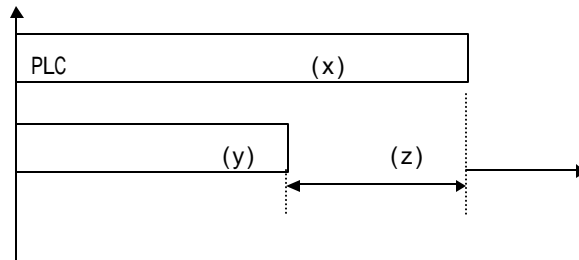
: 가 X: 가

:      ,      1      (16 )      . Fnet      60  
 가      가

		I/O	%IW0.0.0,	%QW0.0.0
--	--	-----	-----------	----------

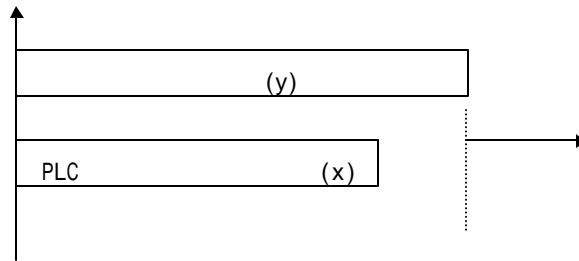


- : 가 PLC  
 ms , (Scan)  
 가  
 20ms 10 가  
 200ms  
 PLC  
 PLC  
 PLC



$$: (z) = (x) - (y) \text{ ms}$$

(a) (PLC > )



$$: (z) = 0 \text{ ms}$$

(b) (PLC < )

[ 6.3.2(F) ] PLC

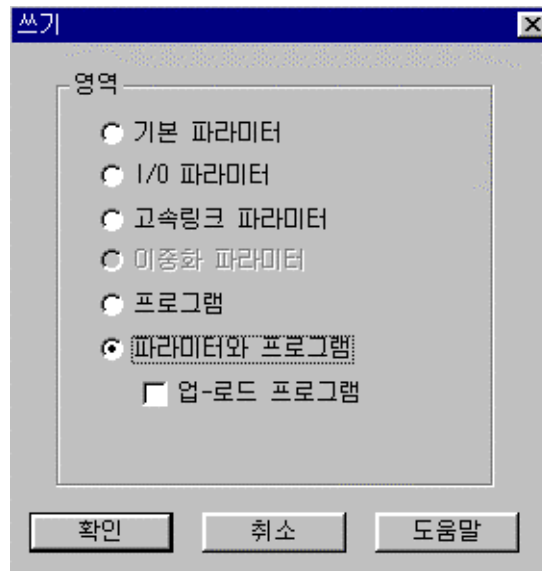
- 1)
  - 2)
- 가

6.3.3

GMWIN

PLC CPU

1)



[ 6.3.3(A) ]

가

GMWIN

, GMWIN

PLC



2)



[ 6.3.3(B) ]

3) G7L-FUEA



가

PLC

가

PLC

PLC CPU

[ 6.3.3 ] PLC

PLC RUN	X	X		
PLC STOP				
PLC PAUSE	X	X		
PLC DEBUG	X	X		

6.3.4

CPU

PLC

(%Q )

CPU

가  
CPU

%M

가 가

6.3.5

GMWIN

가  
(1)

GMWIN

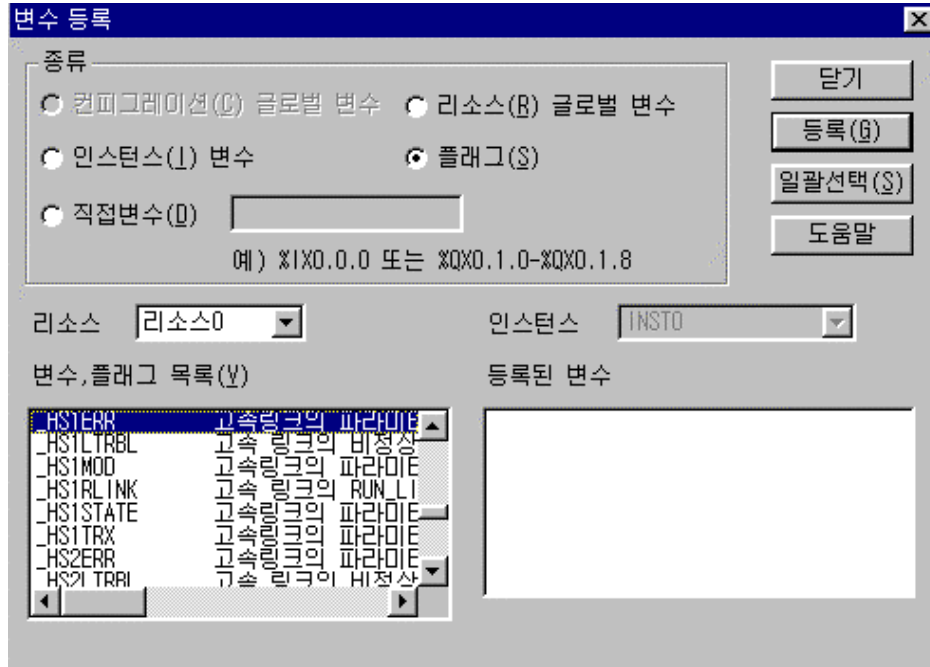
[ 6.3.5(A)]

(\_HSxSTATE[n], \_HSxERR[n], \_HSxMOD[n], \_HSxTRX[n] ARRAY  
가 )

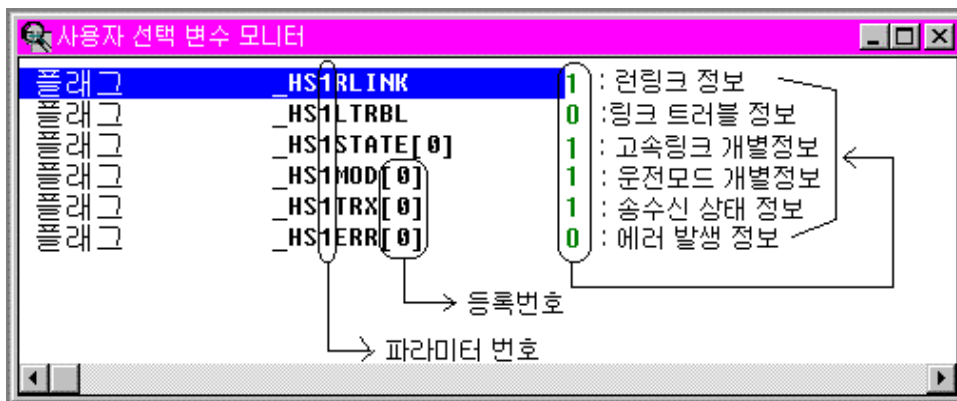
'x' GM1/GM2/GM3 PLC CPU 1 ~ 4  
,GM4,GM6 CPU 1 ~ 2 GM7 1 . [n]  
(0 ~ 63)

[ 6.3.5(A)]

[ 6.3.5(B)]



[ 6.3.5(A) ]



[ 6.3.5(B) ]

( )

6.9

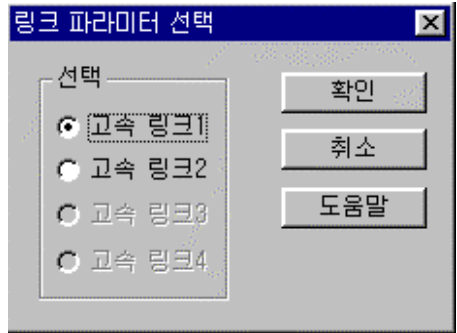
Fnet

(2)

. GMWIN

[ 6.3.5(C) ]

GM4 PLC CPU , 2 가  
 1, 2 가  
 [ 6.3.5(D)]



[ 6.3.5(C)]

[ 6.3.5(D)] - , - 가  
 ( ), ( ),  
 가 .

고속 링크 파라미터 모니터

런 링크: 1 링크 트러블: 0 → 고속링크 종합정보 → 고속링크 파라미터

번호 타입 송수신주기 읽을영역 저장영역 크기 모드 통신 에러 → 고속링크 개별정보

번호	타입	송수신주기	읽을영역	저장영역	크기	모드	통신	에러
0	L24.S0	D(200ms)	%MW0		4	1	1	0
1	L24.S1	D(200ms)	%QW0.1.0		4	1	1	0
2	L24.S2	D(200ms)	%QW0.0.0		4	1	1	0
3	L24.S3	D(200ms)	%QW1.0.0		4	1	1	0
4	L24.S4	D(200ms)	%MW100		2	1	1	0
5						0	0	0
6						0	0	0
7						0	0	0
8						0	0	0
9						0	0	0
10						0	0	0
11						0	0	0
12						0	0	0

Annotations:  
 - word단위 ← (points to size column)  
 - 송신 영역번지 → (points to read/write area)  
 - 통신 주기 → (points to cycle column)  
 - 블럭번호 → (points to address column)  
 - 송신 국번 → (points to station number column)

[ 6.3.5(D)]

( )

[ 6.3.5(D)]

\_\_\_\_\_ : 1 : (24 ) 가 'On' / (RUN) ,  
 가 0 , 1 , 2 , 3 , 4  
 가 ' 0 '

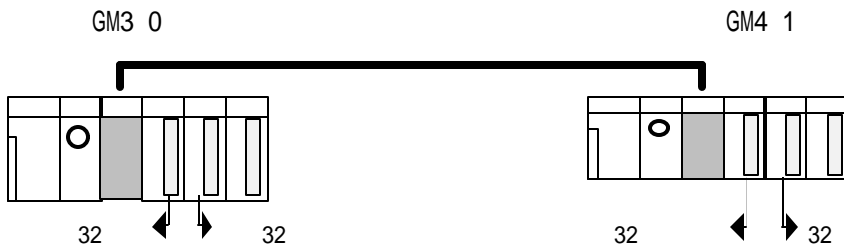
\_\_\_\_\_ : 0 : 가 0 , 1 , 2 , 3 , 4  
 0 ~ 4  
 가 , - 가 'On'  
 ' 1 '

\_\_\_\_\_ 1 : (24 ) RUN ,  
 가 STOP/PAUSE/DEBUG ' 0 '

\_\_\_\_\_ 1 :  
 \_\_\_\_\_ 0 : 가

6.3.6 1) : Fnet PLC

1
GM3/GM4 0 , 1 32 , 2 32 , GM3 32 (%IW0.2.0) GM4 %MWO , GM4 32 (%IW0.2.0) GM3 %MW100



1) [ 6.3.6] I/O CPU

[ 6.3.6] I/O

		I/O ( )				
GM3 (0 )	TX : --> GM4	0 : 1 : OUT 32 2 : IN 32	%IWO.2.0		0	2
	RX : <-- GM4			%MW100	1	2
GM4 (1 )	TX : --> GM3		%IWO.2.0		1	2
	RX : <-- GM3			%MWO	0	2

(GM3,GM4 )

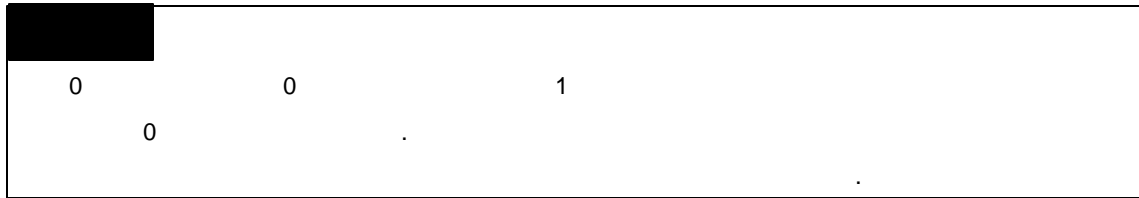
- 1)
- 2) ( ).
- 3) [ 6.3.6]
- 4) GMWIN
- 5)
- 6)
- 7)
- 8)
- 9) 가 On
- 10) 1)

(1) GM3 0

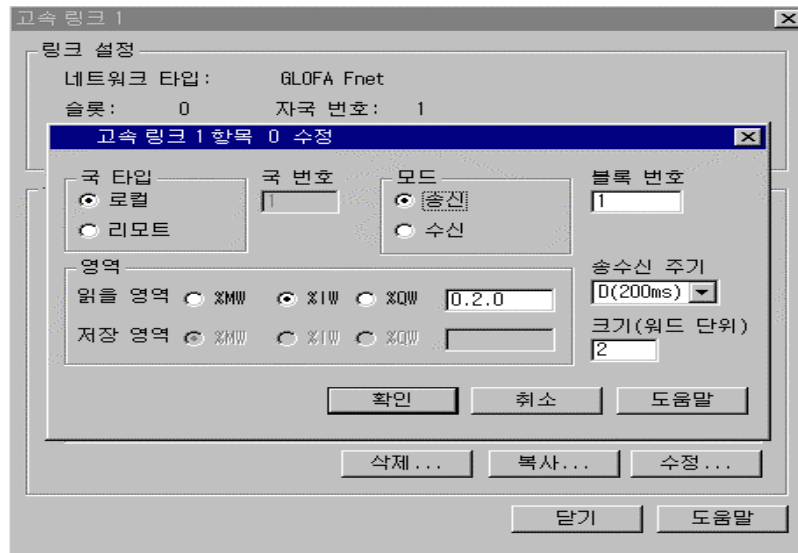




(2) GM3 0



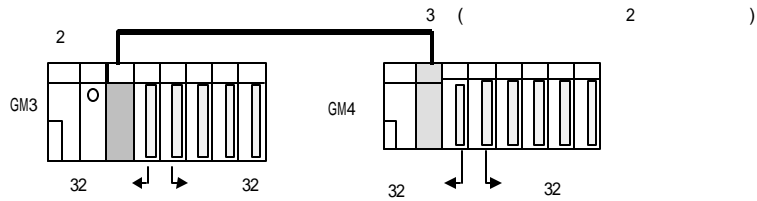
(3) GM4 1





6.3.7 2) : Fnet + I/O .

2	[ 6.3.7]
GM3	(%IWO.1.0) GM4 (%QWO.0.0)
GM4	(%IWO.1.0) GM3 (%QWO.2.0)



[ 6.3.7] Fnet / .

[ 6.3.7]

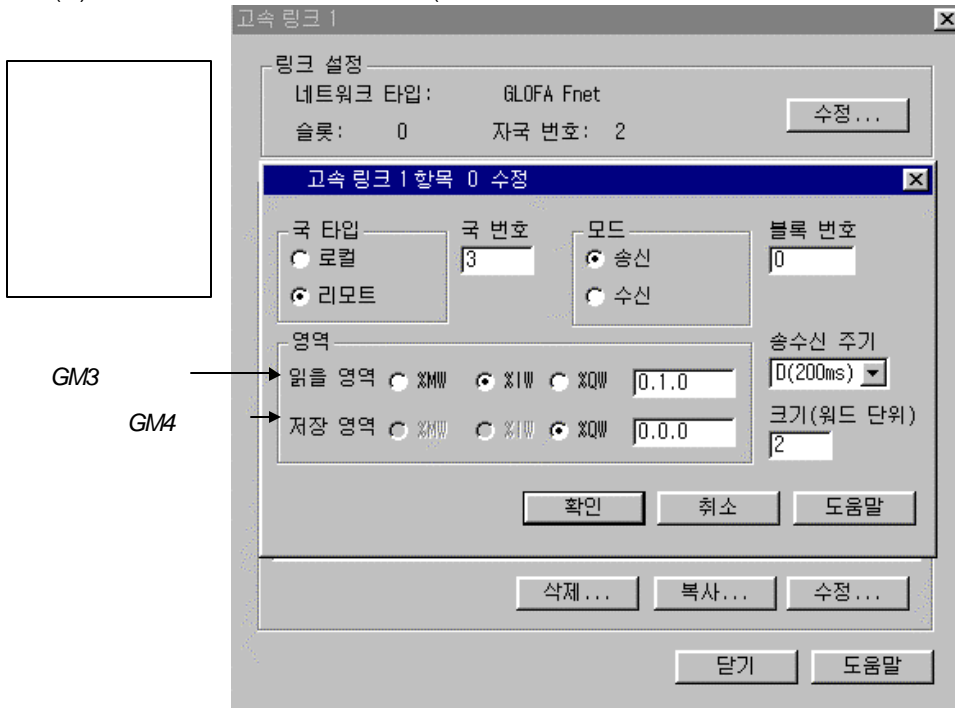
				( )	
GM3	TX: -->GM4	%IWO.1.0(GM3)	%QWO.0.0(GM4)	2(32 )	0
2	RX: <--GM4	%IWO.1.0(GM4)	%QWO.2.0(GM3)	2(32 )	1

I/O GM3 0 : Fnet  
 1 : 32  
 2 : 32

GM4 0 : 32  
 1 : 32

0

(1) GM3 2 (GM3 GM4)

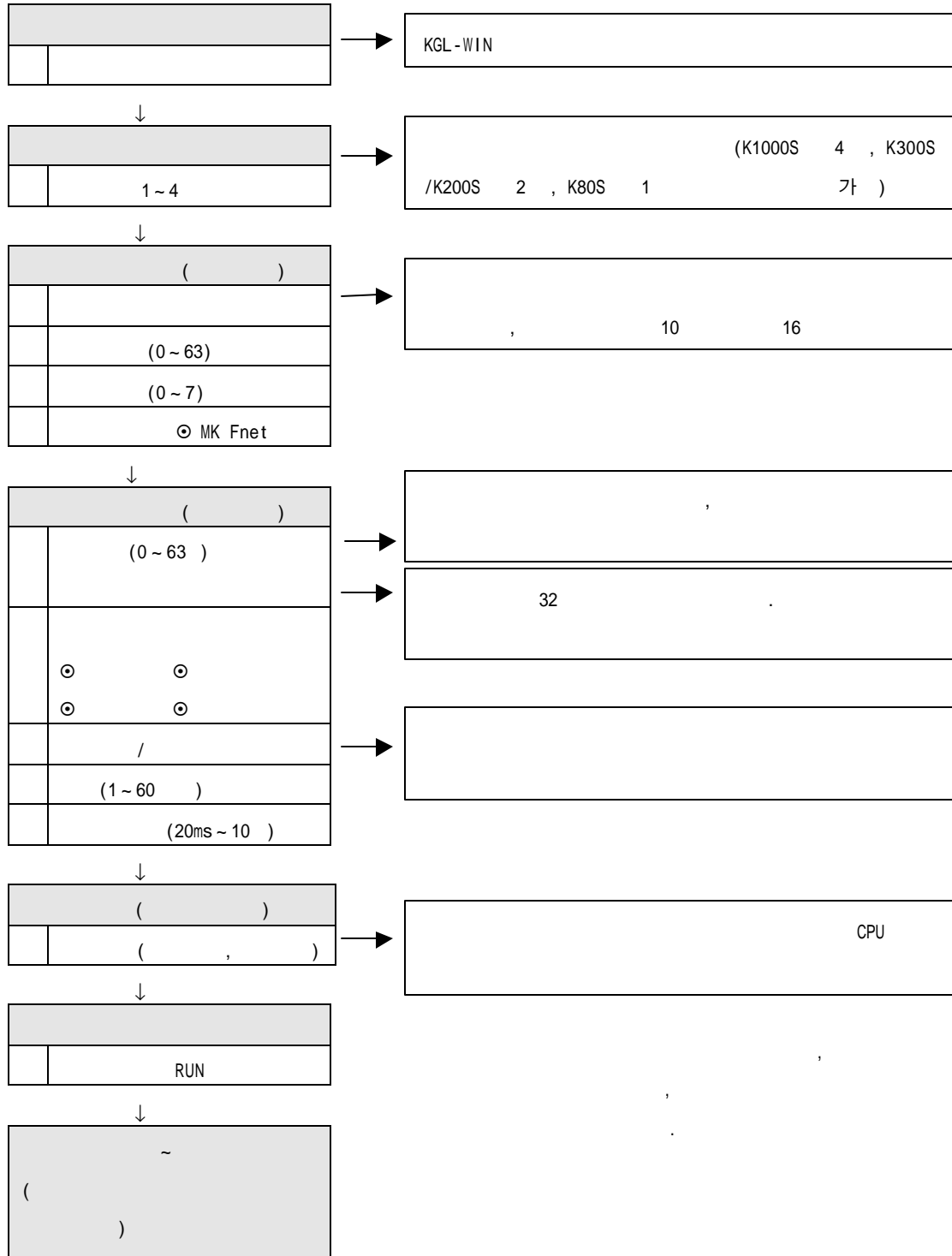


(2) GM3 2 (GM4 GM3)



## 6.4 MASTER-K

### 6.4.1

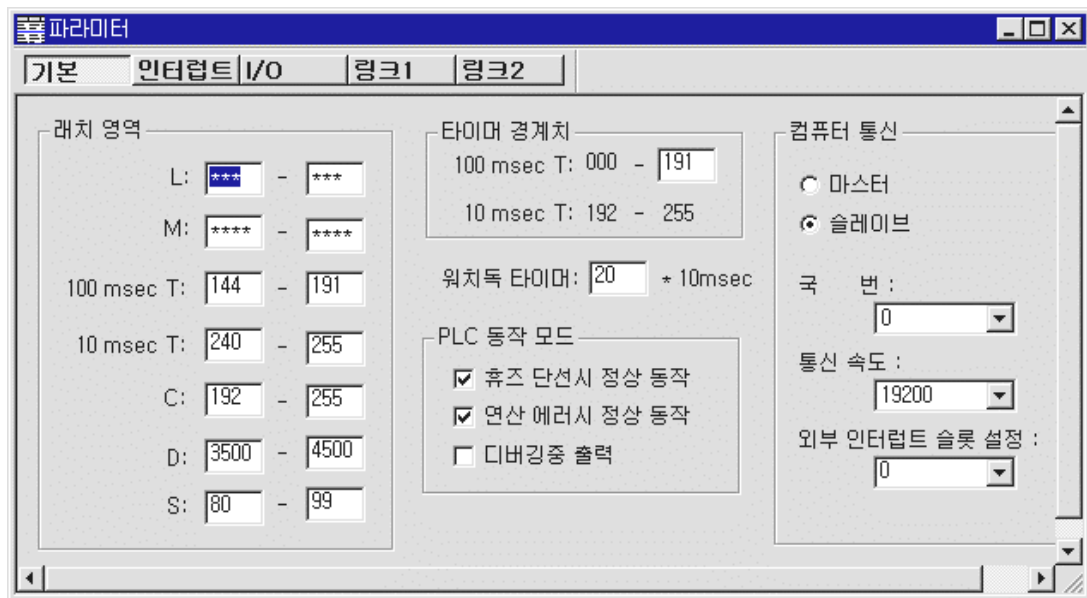


## 6.4.2

KGL-WIN

(1) KGL-WIN

[ 6.4.2(A) ]



[ 6.4.2(A) ] KGL-WIN (K200S )

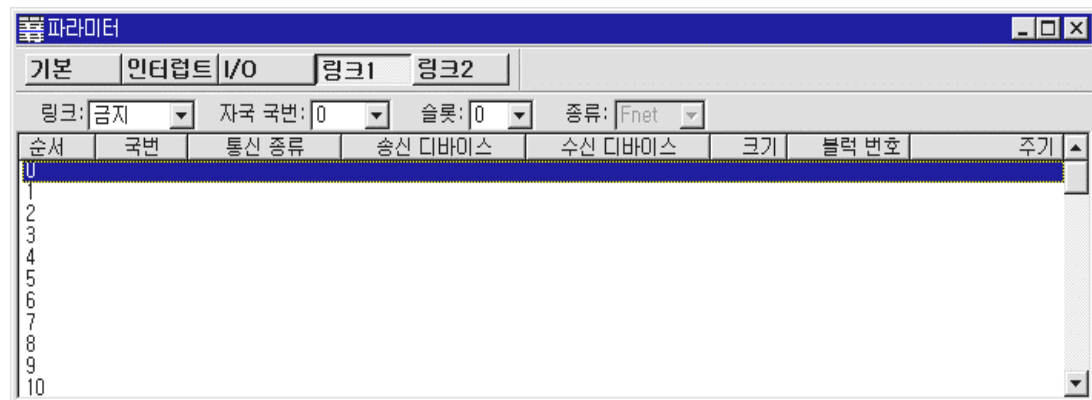
(2)

[ 6.4.2(A) ] KGL-WIN

1

[ 6.4.2(B) ]

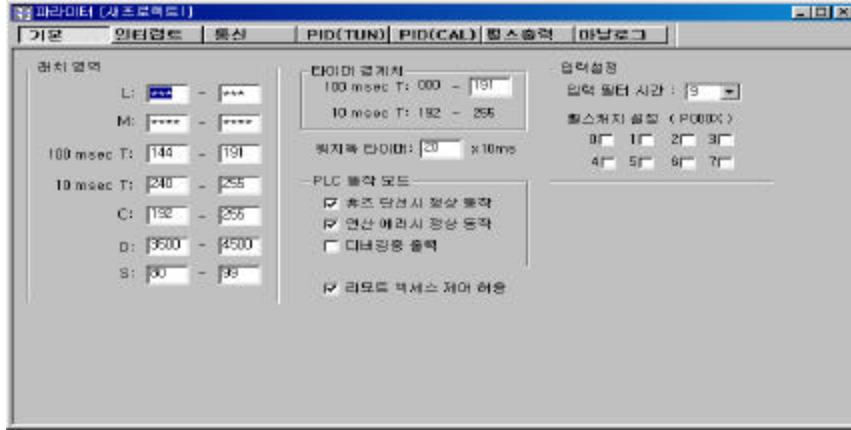
1



[ 6.4.2(B) ]

(3) K80S

[ 6.4.2(C) ] K80S



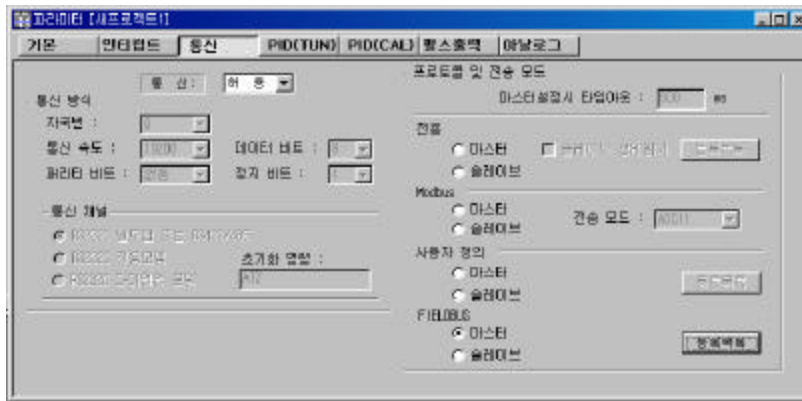
[ 6.4.2(C) ] KGL-WIN (K80S )

[ 6.4.2(C) ] KGL-WIN

[ 6.4.2(D) ]

FIELDBUS

[ 6.4.2(E) ]



[ 6.4.2(D) ]



[ 6.4.2(E) ]

1 : K1000S CPU 4 , K300S/K200S 2 , K80S  
 1  
 가 , 가 . [ 6.4.2(A)] CPU 가 .

[ 6.4.2(A)] CPU

	가		
K1000S	G3L-FUEA/FUOA	4	가 .
K300S	G4L-FUEA/FUOA	2	
K200S	G6L-FUEA	2	
K800S	G7L-FUEA	1	

: .( , )  
 : '0'  
 '63' ,  
 : , '0' '7'  
 : 가 '0'  
 '63' 64 ,

(4)

[ 6.4.2(B)] No.0 , [ 6.4.2(F)] .

[ 6.4.2(F)] ( 1 0 )



: ,  
 ,  
 . [ 6.4.2(B)] .

[ 6.4.2(B)]

		0 ~ 63
	( )	
	( )	

: /

가

0 31 32 가 , 32  
 가 , 32 가 ,  
 32  
 가 . Fnet 64  
 가 64 32

: ,  
 ,  
 : ( )  
 : ( )  
 :  
 :

/ : , /  
 , (P )

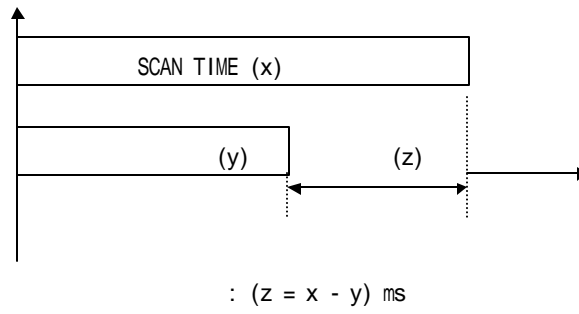
[ 6.4.2(C) ] /

		가	
		P, M, L, K, F, D, T, C	
		P, M, L, K, D, T, C	
		P, M, L, K, F, D, T, C	
		P	
		P	
		P, M, L, K, D, T, C	

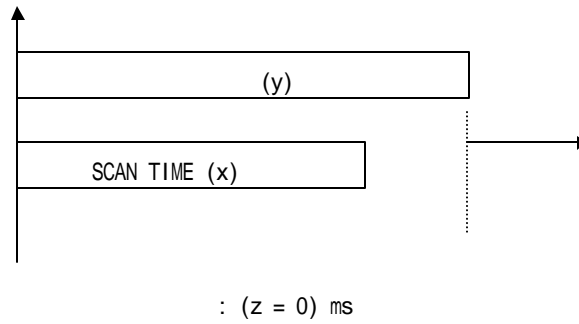
가 : [ 1 (16 ) ], 60  
가 . , 가

가 PLC  
PLC ms  
가 가  
, 20ms(Fnet V2.0 : )  
10 .

200ms 200ms  
PLC PLC  
PLC 가  
'On' , 'Off' - TRX\_MODE



(a) PLC



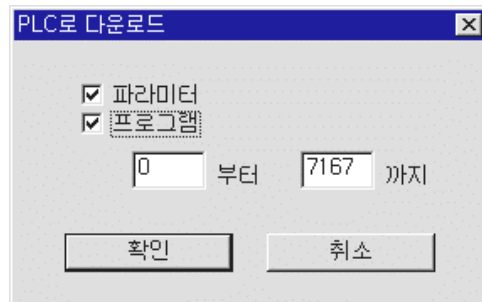
(b) PLC

[ 6.4.2(G) ] PLC

6.4.3

, [ 6.4.2(F) ]

. [ 6.4.3(A) ]



[ 6.4.3(A) ]

가 PLC 가 STOP 가 ,  
 PLC CPU [ 6.4.3(A)]  
 PLC MODE

[ 6.4.3(A)] PLC

RUN	X	0	PLC
STOP	0	0	
PAUSE	X	0	
DEBUG	X	0	

(1)

KGL-WIN

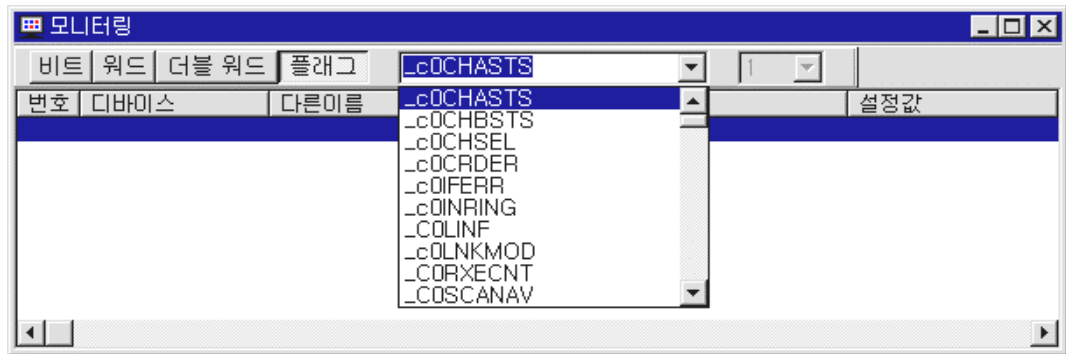
가

(가)

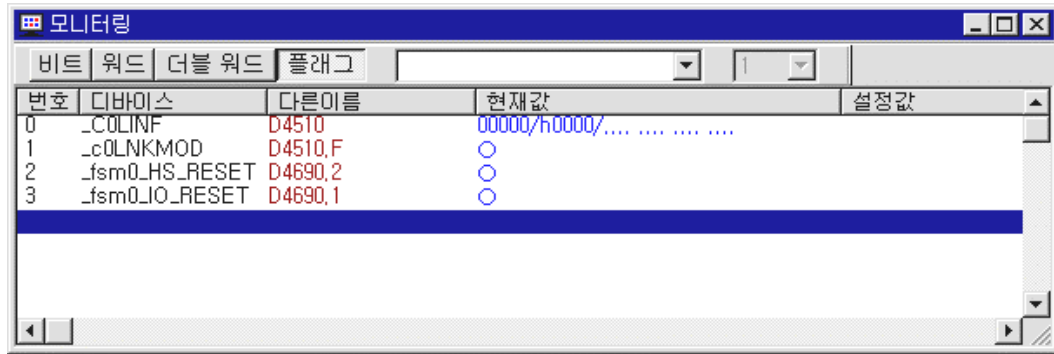
KGL-WIN

6.4.3(B)] , (▼) [

6.4.3(B)] [ 6.4.3(B)]  
 가



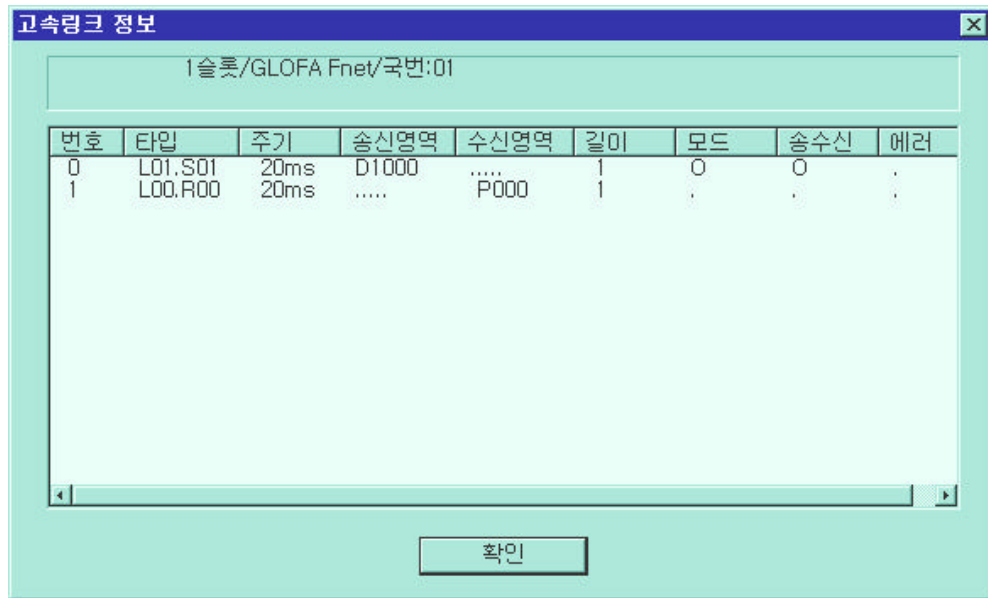
[ 6.4.3(B)]



[ 6.4.3(C) ( 가 ) ]

( )

[ 6.4.3(D) ]



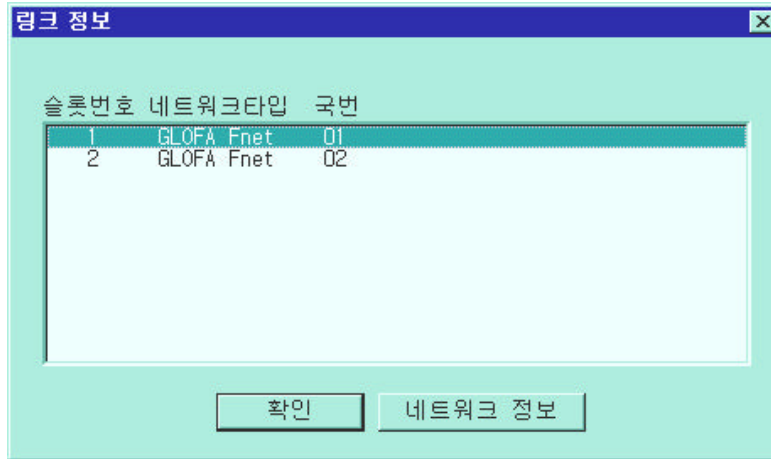
[ 6.4.3(D) ]

0 L01.S01 Local 01 Send 01 , (D1000)

1 Local , L00.R00 Local 00 Receive

00 , 0 Local P0

( )

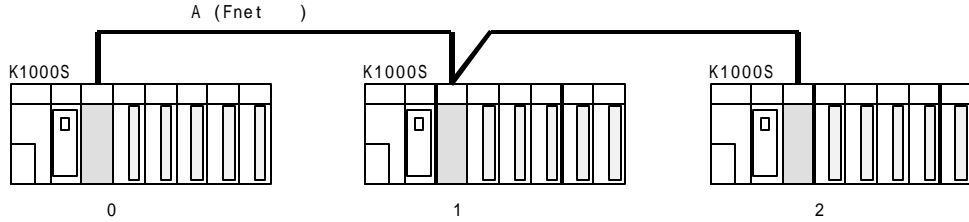


Fnet

.(K80S )

6.4.4 1) Fnet PLC

[ 6.4.4(A) ] Fnet [ 6.4.4(A) ] I/O



[ 6.4.4(A) ] Fnet

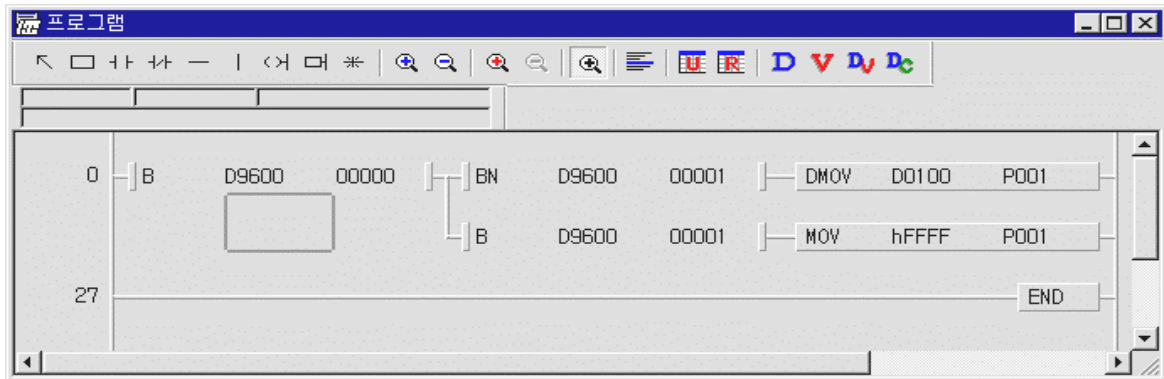
[ 6.4.4(A) ] I/O

		I/O ( )		
K1000S	:-> K1000S(1 )	0 :	P3,P4	-
(0 )	:<-- K1000S(2 )			D0100
K1000S	:-> K1000S(2 )	1 :	32	P3,P4
(1 )	:<-- K1000S(0 )	2 :	32	-
K1000S	:-> K1000S(0 )			P3,P4
(2 )	:<-- K1000S(1 )			-
K1000S CPU		2	(P3, P4)	2
		D0100, D0101	1	(P1, P2)

6.4.4(B) [ 6.4.4(C) ]

(K200S/K300S Fnet

(가)



[ 6.4.4(B) ] 1

[ 6.4.4(B) 가 (RUN\_LINK=1, LINK\_TRUBLE=0) (D0100, D0101) 1 , 가 (LINK\_TRUBLE=1) hFFFF . (RUN\_LINK, LINK\_TROUBLE) 6.1.5(??)

( )

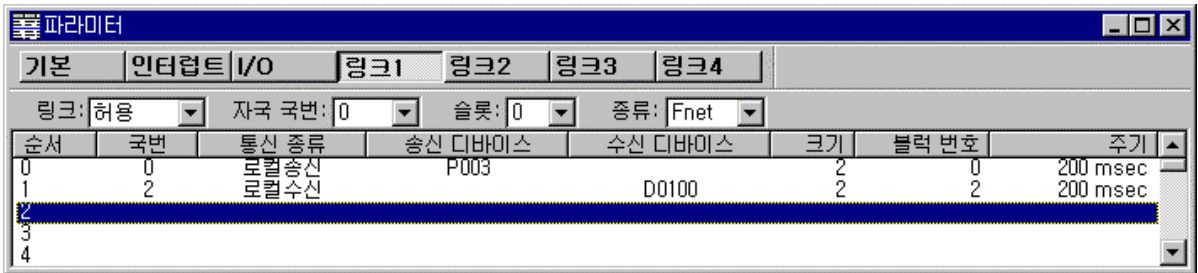
[ 6.4.4(A) 0,1,2 [ 6.4.4(A)]

[ 6.4.4(B)]

[ 6.4.4(A)]

PLC

- 1)
- 2) ( ) .
- 3)
- 4) KGL-WIN
- 5)
- 6)
- 7)
- 8) 1)
- ( 1)



(A) K1000S (0 )



(B) K1000S (1 )



파라미터								
기본		인터럽트		I/O	링크1	링크2	링크3	링크4
링크:	허용	자국 국번:	2	슬롯:	0	종류:	Fnet	
순서	국번	통신 종류	송신 디바이스	수신 디바이스	크기	블럭 번호	주기	
0	2	로컬송신	P003		2	2	200 msec	
1	1	로컬수신		D0100	2	1	200 msec	
2								
3								
4								

(C) K1000S (2 )

[ 6.4.4(C)]

( )

1)

3

2

6.2.4

$$St = P\_scanA + C\_scan + P\_scanB$$

$$St =$$

$$P\_scanA = PLC A$$

$$P\_scanB = PLC B$$

$$C\_scan =$$

P\_scanA, P\_scanB K1000S PLC

5ms

가 (KGL-WIN - -PLC 가 )

$$Cscan = Th \times Sn \text{ (Th = Token Hold Time : 1 token)}$$

$$Sn = \text{Total Station Number : } ( )$$

$$= 8ms \times 3$$

$$= 24ms$$

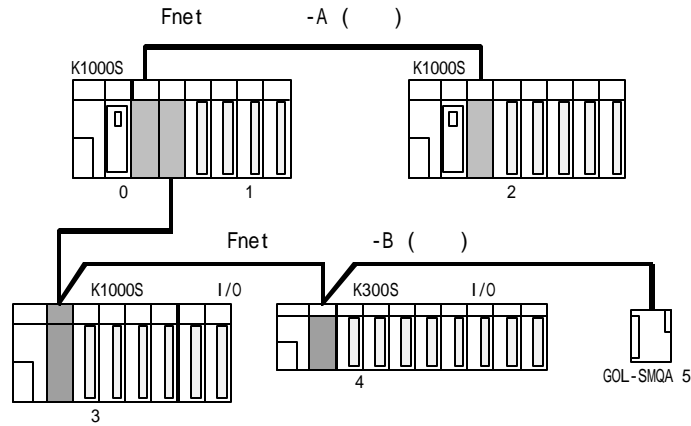
$$St = P\_scanA(=5ms) + P\_scanB(=5ms) + Cscan(24ms) = \underline{34ms}$$

34ms

6.4.5 2) Fnet + + I/O

(가)

[ 6.4.5(A) ] Fnet -A/B PLC  
I/O



[ 6.4.5(A) ] Fnet /

-A , -B  
I/O 0 2  
-A -B 1  
K1000S-CPU( 0 ) K1000S-CPU( 2 ) 1  
-B 3 /4 5 ( )  
1 ) 3 /4 /5  
3 /4 5 1 Dip-Switch  
[ 6.4.5(A) ] [ 6.4.5(A) ]  
I/O

[ 6.4.5(A)] I/O

PLC Type	I/O	Local/Remote		
K1000S CPU (0, 1)	0: (0) --> A 1: (1) --> B	Local : (2) Remote : 3(3) Remote : 4(4) Remote : (5)	D1000 D1100 D0000 D0010 D0200	D1000 D1100
K1000S CPU (2)	0: (2) --> A	Local : (0)		D0000
K1000S	0: 32 1: 32	Local : K1000S(1)	P0, P1	P2, P3
K300S	0: 16 1: 16	Local : K1000S(1)	P0, P1	P2, P3
Single-Remote	16	Local : K1000S(1)	P0, P1	

( )

[ 6.4.5(A)] 1 3,4,5 I/O ,  
 D0000, D0100, D0200 K1000S- , K300S- ,  
 I/O P0,P1 , K1000S- . K300S- P2,P3  
 D1000, D1100 , -A K1000S-CPU 2  
 K1000S- , K300S- , I/O  
 1 I/O  
 가 (K1000S-CPU  
 1 ) , [ 6.4.5(B)] -A/B  
 CPU K1000S 가  
 K1000S  
 Flag RUN\_LINK,  
 LINK\_TROUBLE(\_HSORLINK,\_HSOLTRBL) . [ 6.4.5(B)]

파라미터							
기본		인터럽트 I/O		링크1	링크2	링크3	링크4
링크:	허용	자국 국번:	0	슬롯:	0	종류:	Fnet
순서	국번	통신 종류	송신 디바이스	수신 디바이스	크기	블럭 번호	주기
0	0	로컬송신	D1000		2	0	200 msec
1	0	로컬송신	D1100		2	1	200 msec
2							
3							
4							

(a) -A 0

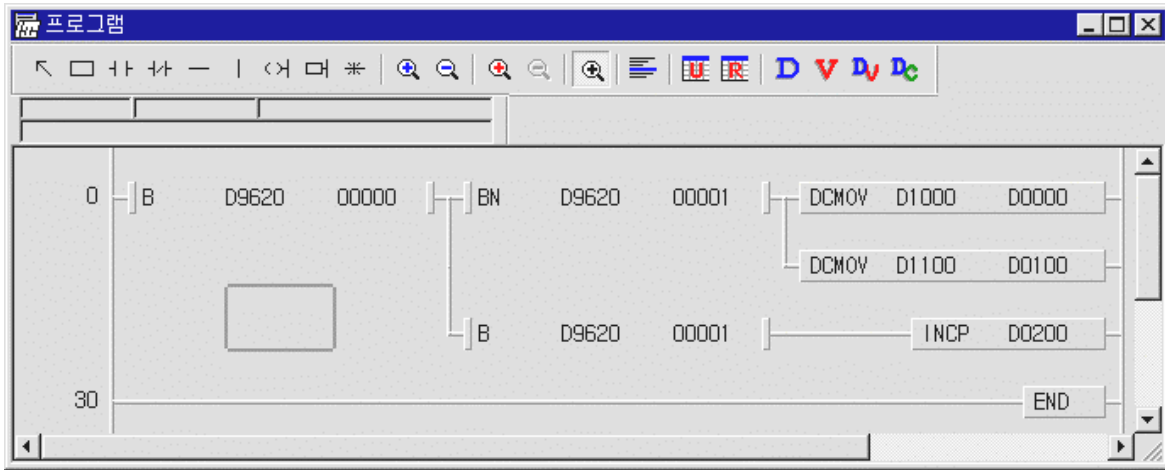
파라미터							
기본		인터럽트 I/O		링크1	링크2	링크3	링크4
링크:	허용	자국 국번:	2	슬롯:	0	종류:	Fnet
순서	국번	통신 종류	송신 디바이스	수신 디바이스	크기	블럭 번호	주기
0	0	로컬수신		D0000	2	0	200 msec
1	0	로컬수신		D0100	2	1	200 msec
2							
3							
4							

(b) -A 2

파라미터							
기본		인터럽트 I/O		링크1	링크2	링크3	링크4
링크:	허용	자국 국번:	1	슬롯:	0	종류:	Fnet
순서	국번	통신 종류	송신 디바이스	수신 디바이스	크기	블럭 번호	주기
0	3	리모트송신	D0000	P000	2	0	200 msec
1	3	리모트수신	P002	D1000	2	1	200 msec
2	4	리모트송신	D0100	P000	2	0	200 msec
3	4	리모트수신	P002	D1100	2	1	200 msec
4	5	리모트송신	D0200	P000	1	0	200 msec
5							
6							

(c) -B 1 3,4,5

[ 6.4.5(B)]



[ 6.4.5(C) ]

[ 6.4.5(C) ] 2) K1000S PLC( 0 )  
 3,4 3,4 , -  
 D0200 , 5  
 , 2

( )

[ 6.4.5(D) ] 3

- 가 On

가

, [ 6.4.5(D) ] \_FSMn\_reset

\_FSMn\_st\_no , \_FSMn\_reset '1'

, '0' n

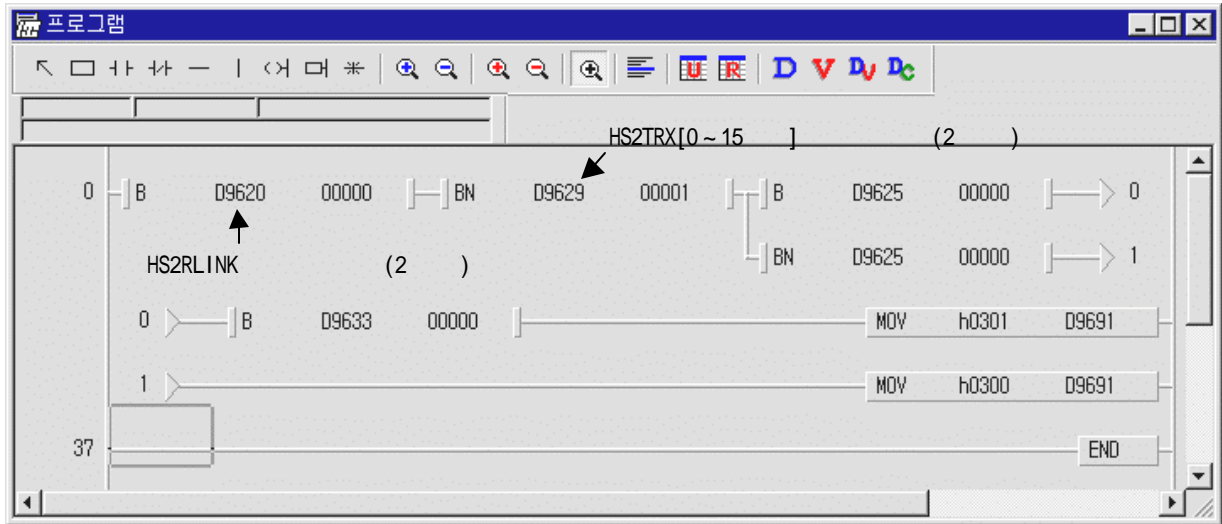
0 7 가 3 - 가

'1' , \_HS2TRX 가 '1' , \_HS2MODE \_HS2ERR '0' 가

\_FSM1\_ST\_NO 3 , \_FSM1\_reset

'1' , \_HS2MODE \_HS2TRX 가 '1' \_FSM1\_reset

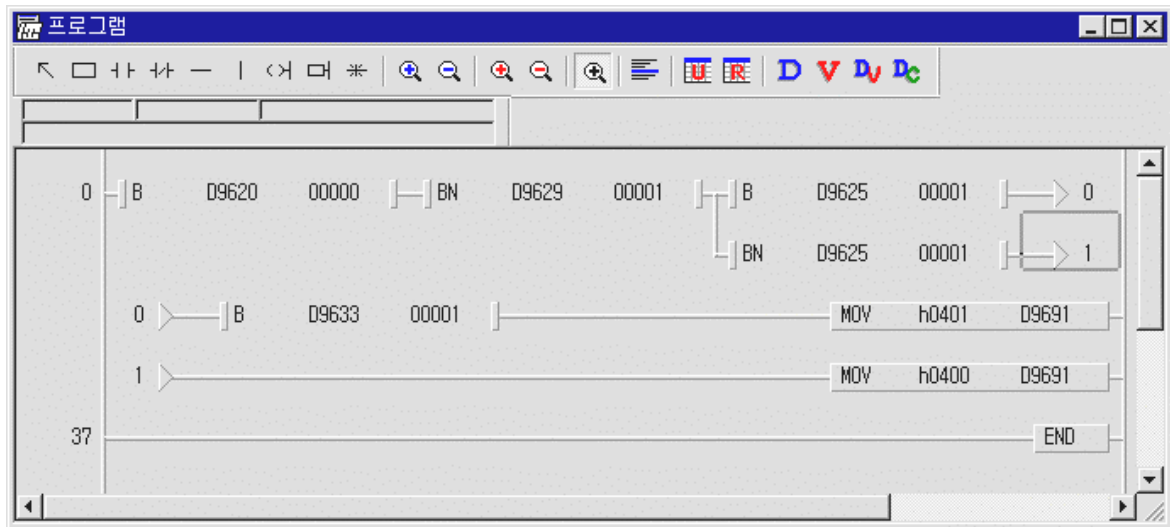
'0'



[ 6.4.5(D) ] 3

( [ ] )

6.4.5(D)] 0,1 [1] . [ 6.4.5(E) ] 4



[ 6.4.5(E) ] 4

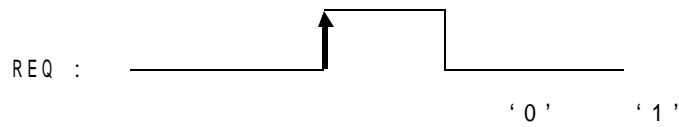


6.5.3.

3가

READ/WRITE	
STATUS	PLC
DA4INI	(            ).

6.5.4

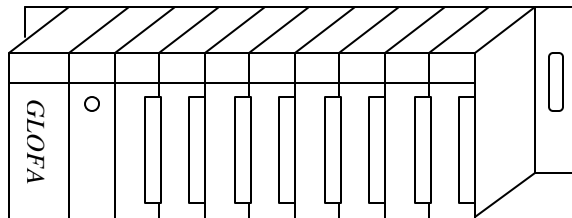


, NDR    ERR    가

NET\_NO :

PLC

CPU    ‘ 0 ’



POWER CPU 0 1 2 3 4 5 6 7

ST\_NOH / ST\_NOL :

Fnet                    /

Rdtype





## 6.5.6

[ 6.4.6]

가

PLC

(0 :

가,

X :

가)

(bit )	PLC	GM1	GM3	GM4	GM6		
		GM2					(RD / WR)
( 4 )	BOOL(1)	0	0	0	0	0	RD(WR)BOOL
	BYTE(8)	0	0	0	0	0	RD(WR)BYTE
	WORD(16)	0	0	0	0	0	RD(WR)WORD
	DWORD(32)	0	0	0	0	0	RD(WR)DWORD
	LWORD(64)	0	X	X	X	X	RD(WR)LWORD
	USINT(8)	0	0	0	0	X	RD(WR)USINT
	UINT(16)	0	0	0	0	X	RD(WR)UINT
	UDINT(32)	0	0	0	0	X	RD(WR)UDINT
	ULINT(64)	0	X	X	X	X	RD(WR)ULINT
	SINT(8)	0	0	0	0	X	RD(WR)SINT
	INT(16)	0	0	0	0	X	RD(WR)INT
	DINT(32)	0	0	0	0	X	RD(WR)DINT
	LINT(64)	0	X	X	X	X	RD(WR)LINT
	REAL(32)	0	X	X	X	X	RD(WR)REAL
	LREAL(64)	0	X	X	X	X	RD(WR)LREAL
	TIME(16)	0	0	0	0	X	RD(WR)TIME
	DATE(48)	0	0	0	0	X	RD(WR)DATE
	TIME of DAY(48)	0	0	0	0	X	RD(WR)TOD
	DATE and TIME(48)	0	0	0	0	X	RD(WR)DT
( Fnet : 120 )		0	0	0	0	0	RD(WR)
( 100 )	BOOL	0	0	0	0	X	RD(WR)
	BYTE	0	0	0	0	X	RD(WR)
	WORD	0	0	0	0	0	RD(WR)
	DWORD	0	0	0	0	X	RD(WR)
	LWORD	0	X	X	X	X	RD(WR)
	USINT	0	0	0	0	X	RD(WR)
	UINT	0	0	0	0	X	RD(WR)
	UDINT	0	0	0	0	X	RD(WR)
	ULINT	0	X	X	X	X	RD(WR)
	SINT	0	0	0	0	X	RD(WR)
INT	0	0	0	0	X	RD(WR)	

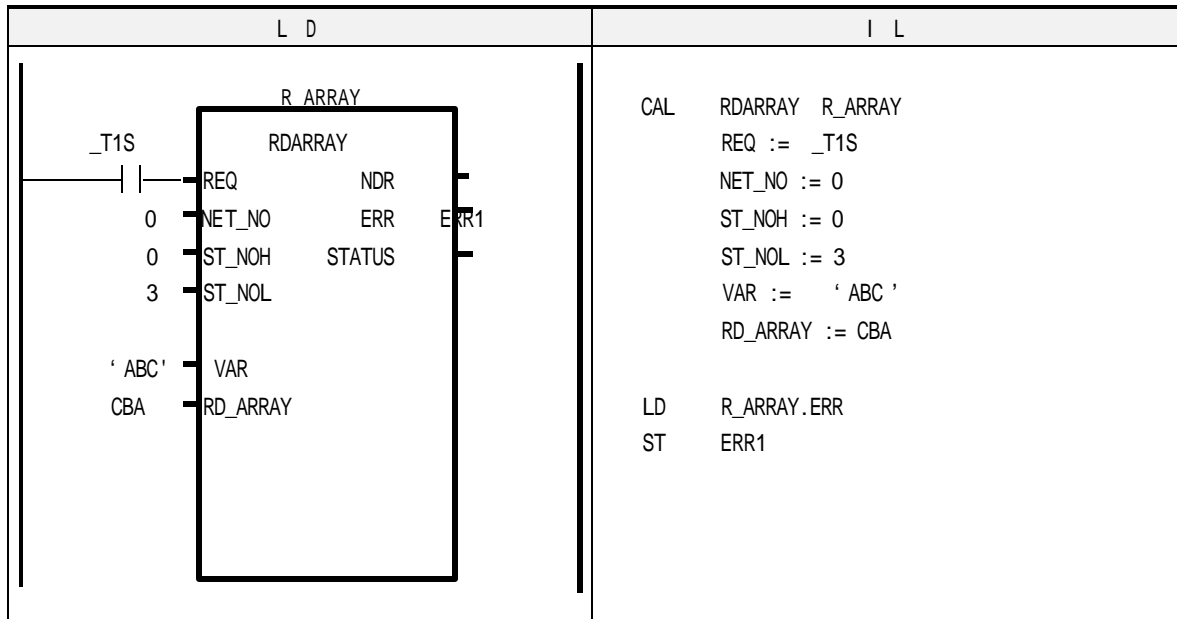
PLC (bit )		GM1	GM3	GM4	GM6		(RD / WR)
		GM2					
( 100 )	DINT	0	0	0	0	X	RD(WR)
	LINT	0	X	X	X	X	RD(WR)
	REAL	0	X	X	X	X	RD(WR)
	LREAL	0	X	X	X	X	RD(WR)
	TIME	0	0	0	0	X	RD(WR)
	DATE	0	0	0	0	X	RD(WR)
	TIME of DAY	0	0	0	0	X	RD(WR)
DATE and TIME	0	0	0	0	X	RD(WR)	



v : Fnet ,0 Fnet 가  
 3 ABC ABC CBA  
 .(3 ABC , REQ 1  
 )

- 3 ( 6.4.8?? )

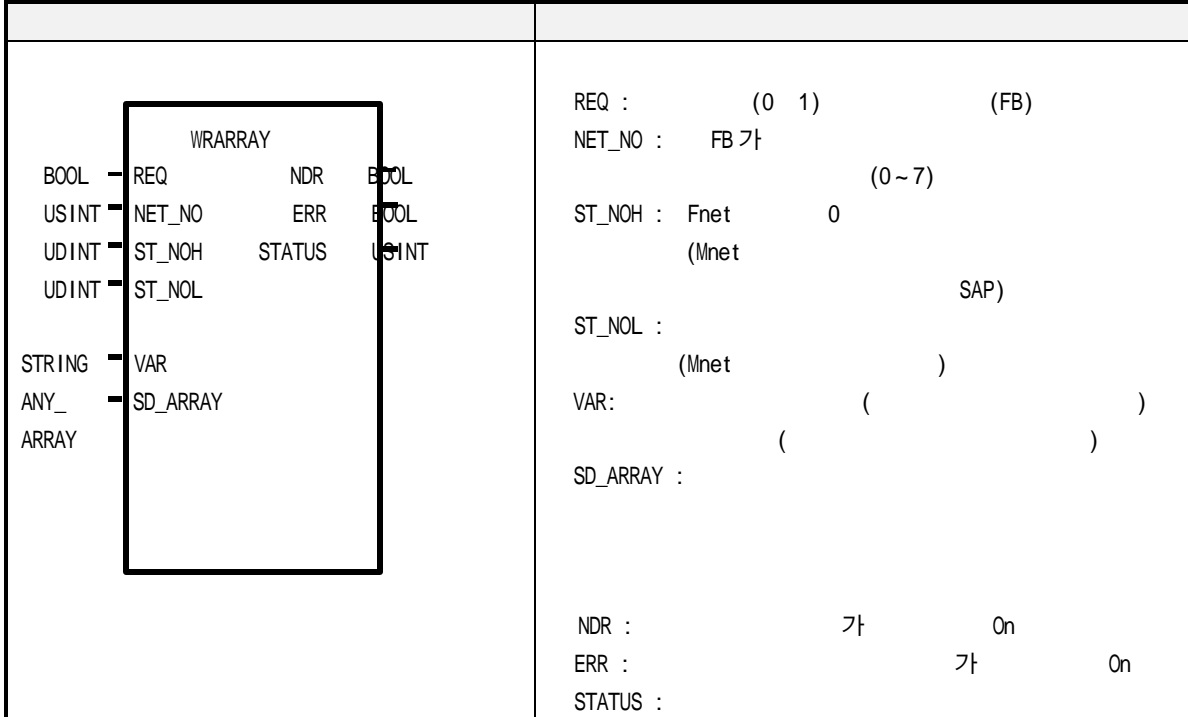
	ABC	DEF( )	ABC DEF
	RES1.DEF	-	DEF



WRARRAY

( 100 )

	GM1	GM2	GM3	GM4	GM6	
가	λ	λ	λ	λ	λ	



v

```

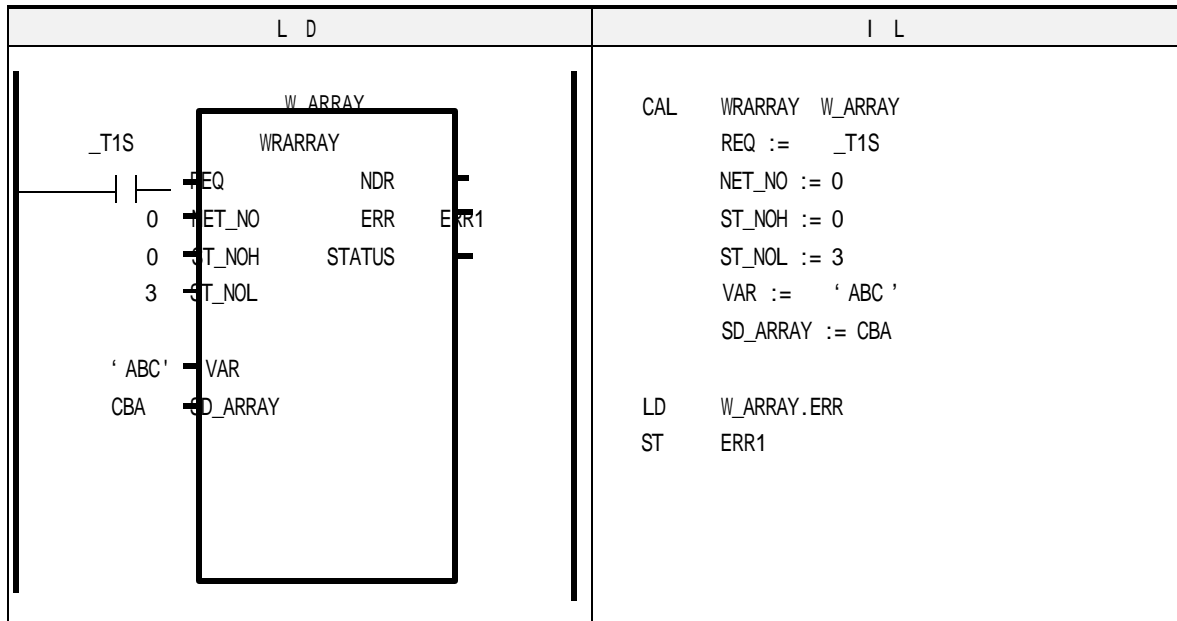
( : %I,%Q,%M )
( 100 ).
v ST_NOH / ST_NOL
( RDTYPE )
v VAR :
( )
v WRARRAY
가
( .)
v NDR / ERR / STATUS
( RDTYPE )

```

v : Fnet ,0 Fnet 가  
 3 ABC CBA  
 (3 ABC , REQ 1  
 )

• 3 ( 6.4.8?? )

	ABC	DEF( )	ABC DEF
	RES1.DEF	-	DEF





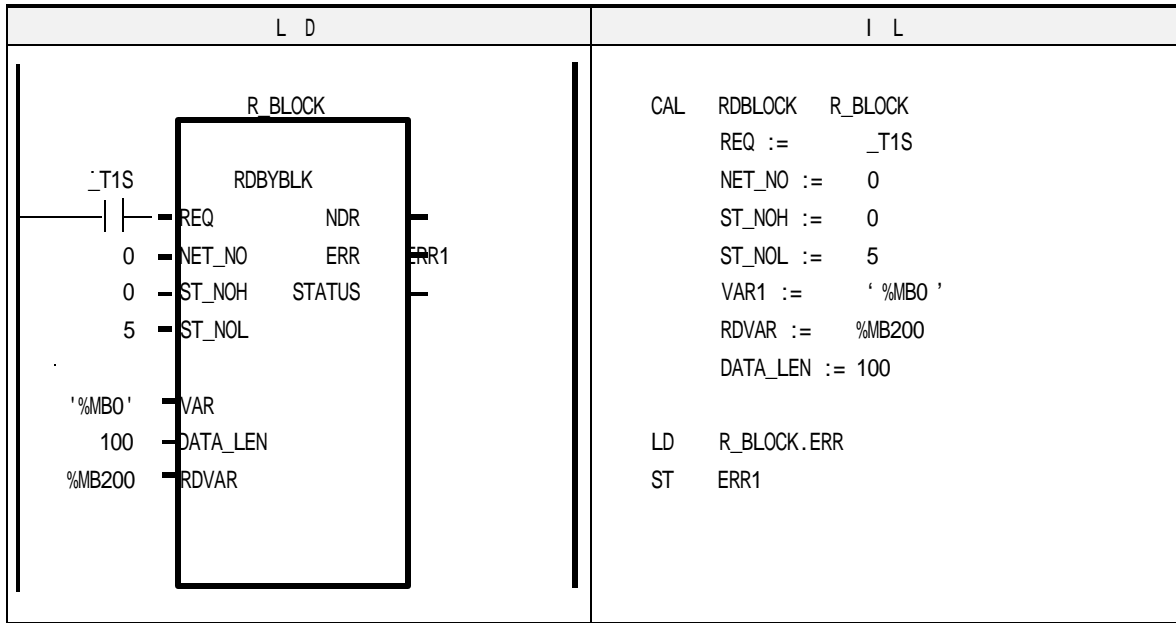


v DATA\_LEN

v NDR / ERR / STATUS

( RDTYPE )

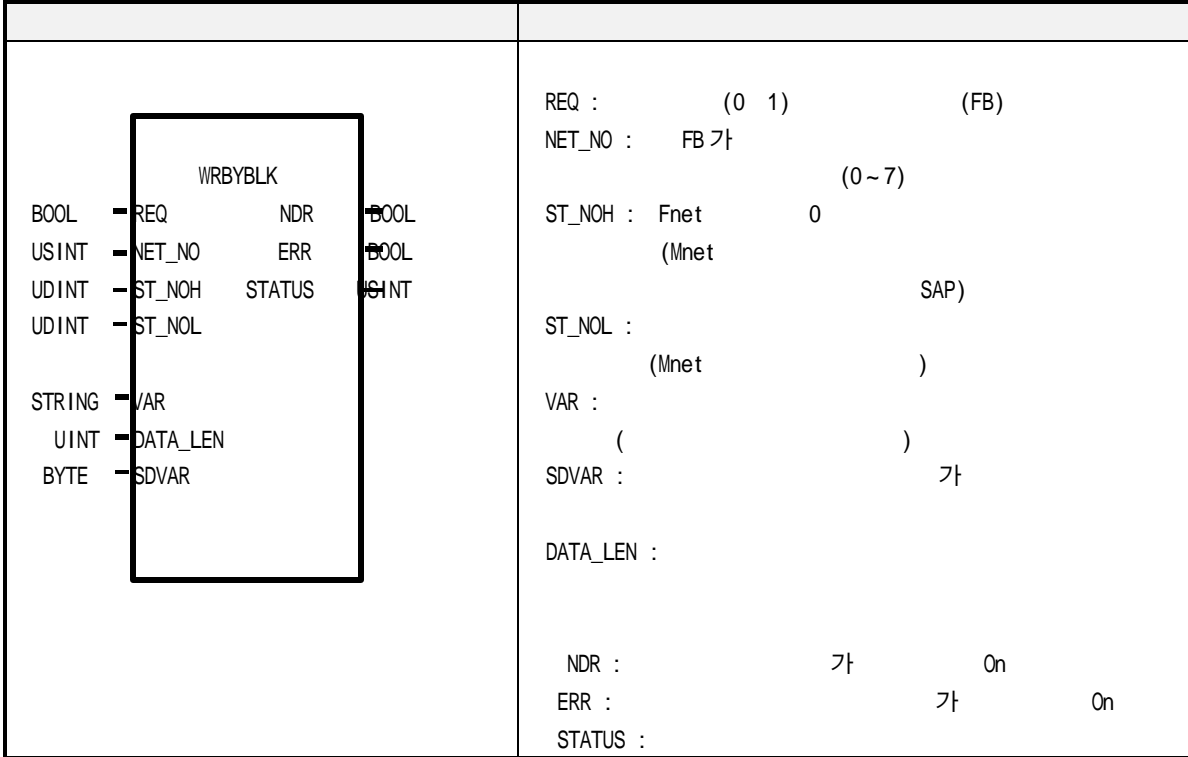
v : Fnet , 0 Fnet 가  
 5 %MBO 100 %MB200 %MB299  
 (REQ 1 ).



WRBLOCK

( : 120 )

	GM1	GM2	GM3	GM4	GM6	
가	λ	λ	λ	λ	λ	



v

(%I,%Q,%M)

v ST\_NOH / ST\_NOL

( RDTYPE )

v VAR

BYTE  
)%MB100 - 100

%IB0.2.1 -	(0)	2	(2)		1
%QB0.3.1 -	(0)	3	(3)		1

v SDVAR

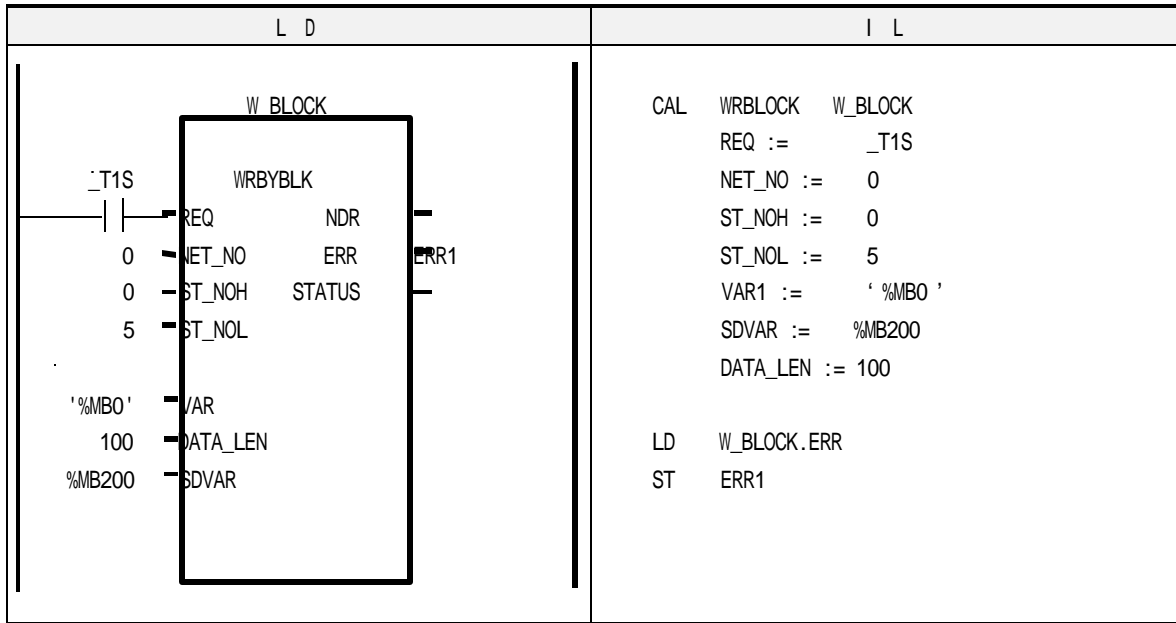
가 ( ).

v DATA\_LEN

v NDR / ERR / STATUS

( RDTYPE )

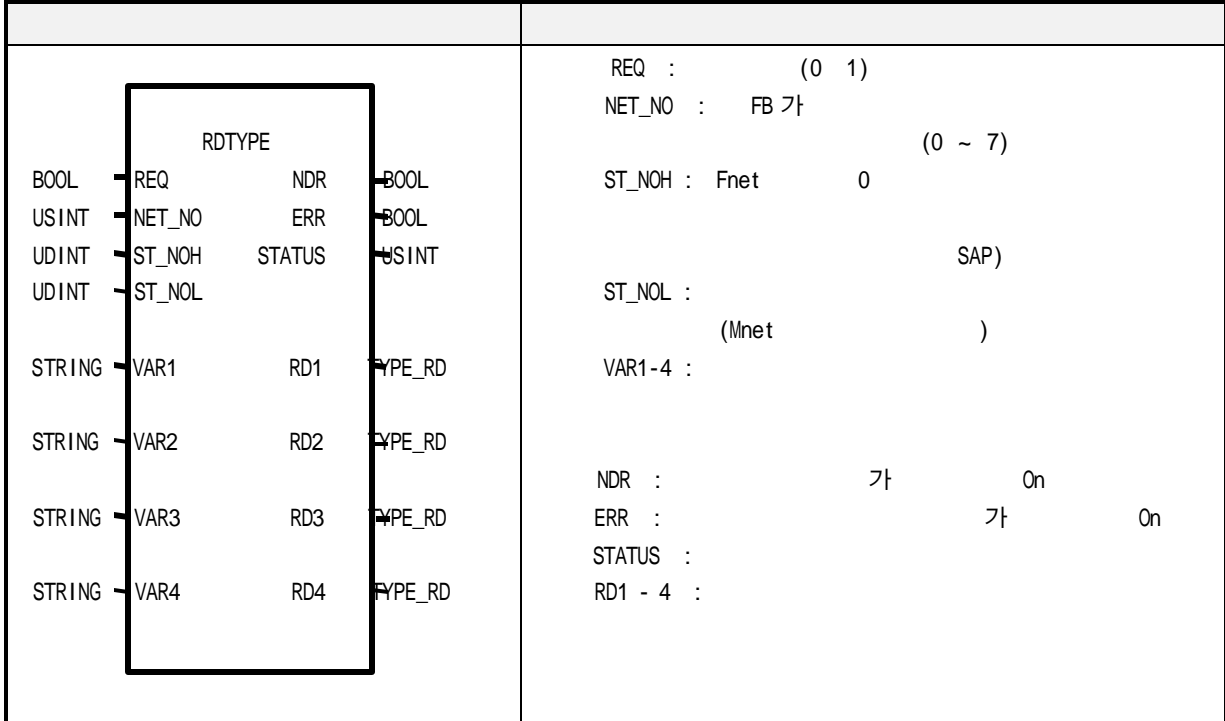
v : Fnet , 0 Fnet 가  
 5 %MB200 %MB299 %MBO %MB99  
 (REQ 1 ).



RDTYPE(BOOL...DT)



	GM1	GM2	GM3	GM4	GM6	
가	λ	λ	λ	λ	λ	



v

) (16Bit)

“ RDWORD ”

v ST\_NOH / ST\_NOL

( ) ,

λ Fnet : ST\_NOH=0( ) , ST\_NOL= ( 10 10 10,16

16#A)

v VAR1 - VAR 4

```

                                (String)
                                .
                                ( "RDWORD"
                                VAR1 - VAR 4
                                (WORD)
                                ).
:
가                                BOOL, BYTE, WORD, DWORD, LWORD(GM1/2).
)                                100                                : '%MX100'
)                                (0) 2                                (2)                                16                                : '%IWO.2.0'
:
6.4.8??                                ).

```

\* VAR1 ~ VAR4

( ' ' ) .

v RD1 - RD4

```

가                                가                                . VAR1                                RD1
가 VAR2,3,4                                RD2,3,4                                .
.

```

v NDR

On Off .

v ERR

```

가                                On
On                                . 가                                .

```

v STATUS

```

가                                ,
                                (                                6-51 ??                                ).

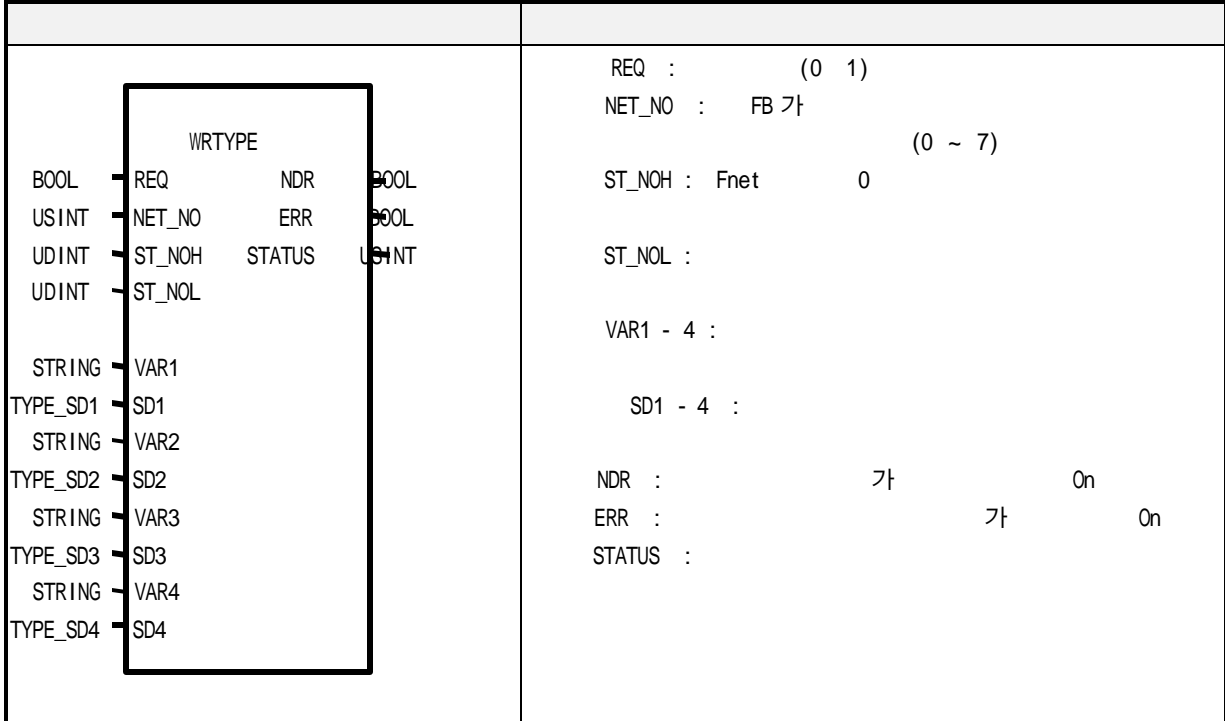
```



WRTYPE(BOOL...DT)



	GM1	GM2	GM3	GM4	GM6	
가	λ	λ	λ	λ	λ	



v

) (8 ) "WRBYTE"

"RDTYPE"

v ST\_NOH / ST\_NOL

( )

v VAR1 - VAR 4

(String)

( "WRBYTE"

(BYTE)

- VAR1 ~ VAR4 ( ' ' )

v SD1 - SD4

, 가 SD2,3,4 . SD1 VAR1  
R2,3,4 .

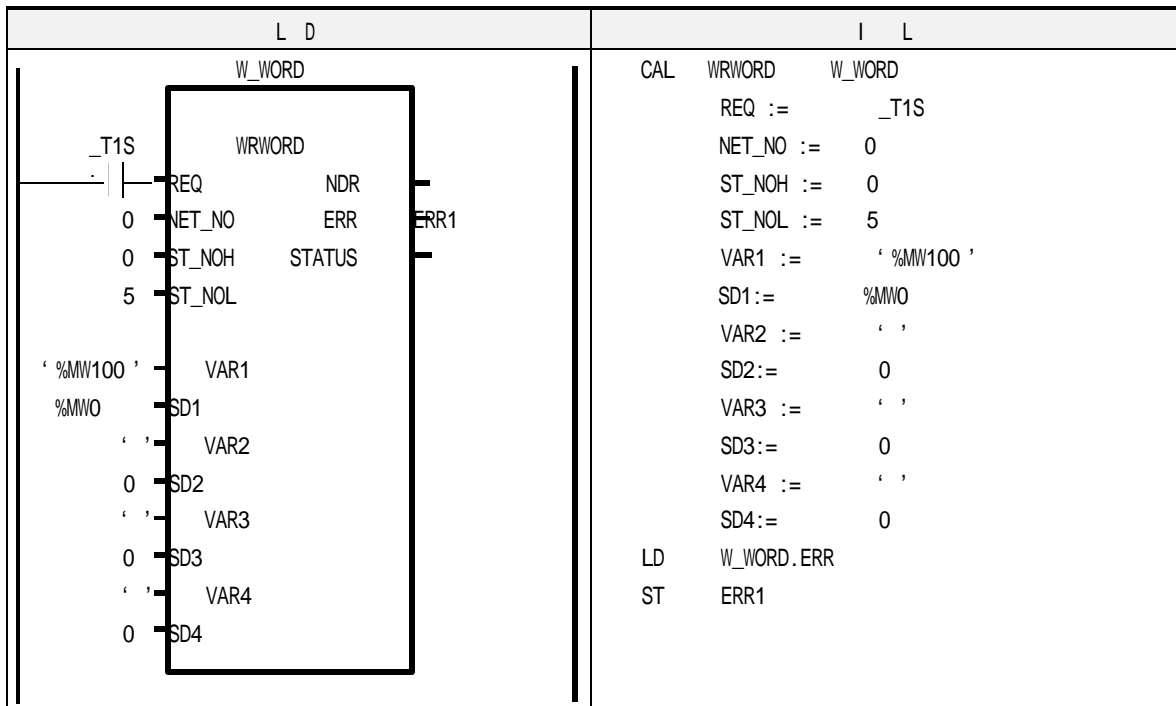
\* SD1 - SD4 0 .

v NDR / ERR / STATUS

“ RDTYPE ”

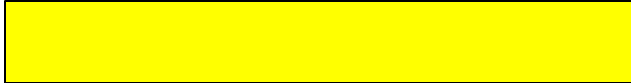
v : Fnet ,0 Fnet 가

(WRWORD REQ 1 )  
%MWO 5 %MW100

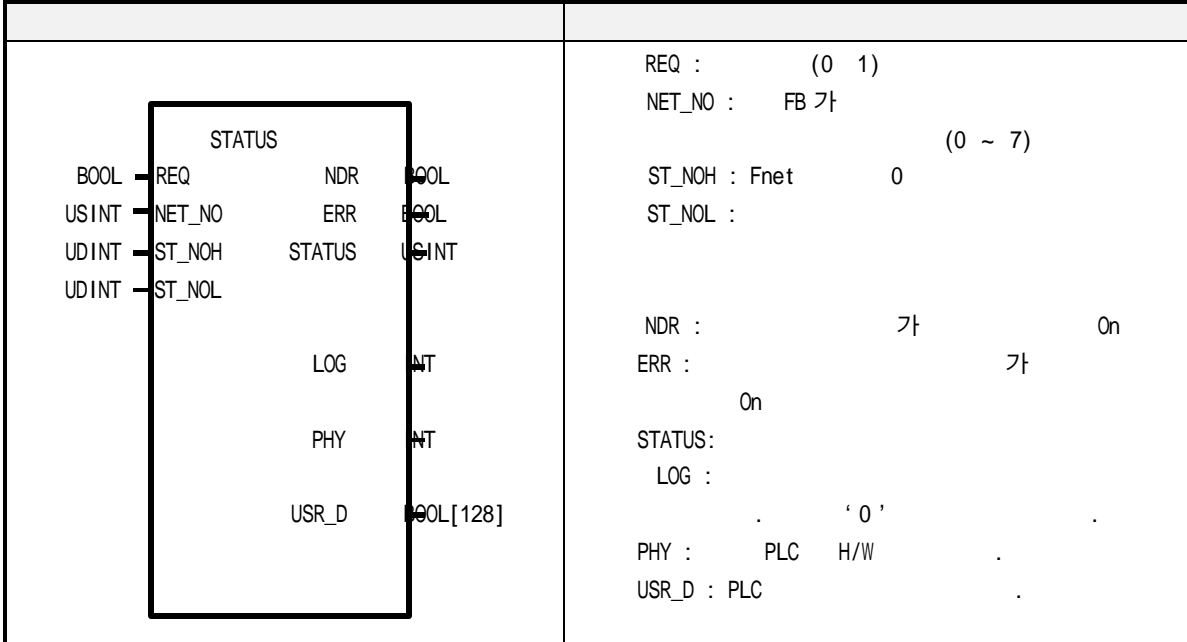




STATUS



	GM1	GM2	GM3	GM4	GM6	
가	λ	λ	λ	λ	λ	



v

v ST\_NOH / ST\_NOL  
( RDTYPE )

v LOG  
(Logical State)

0 = STATE-CHANGE-ALLOWED

v PHY

Physical State PLC H/W

0 = OPERATIONAL( )

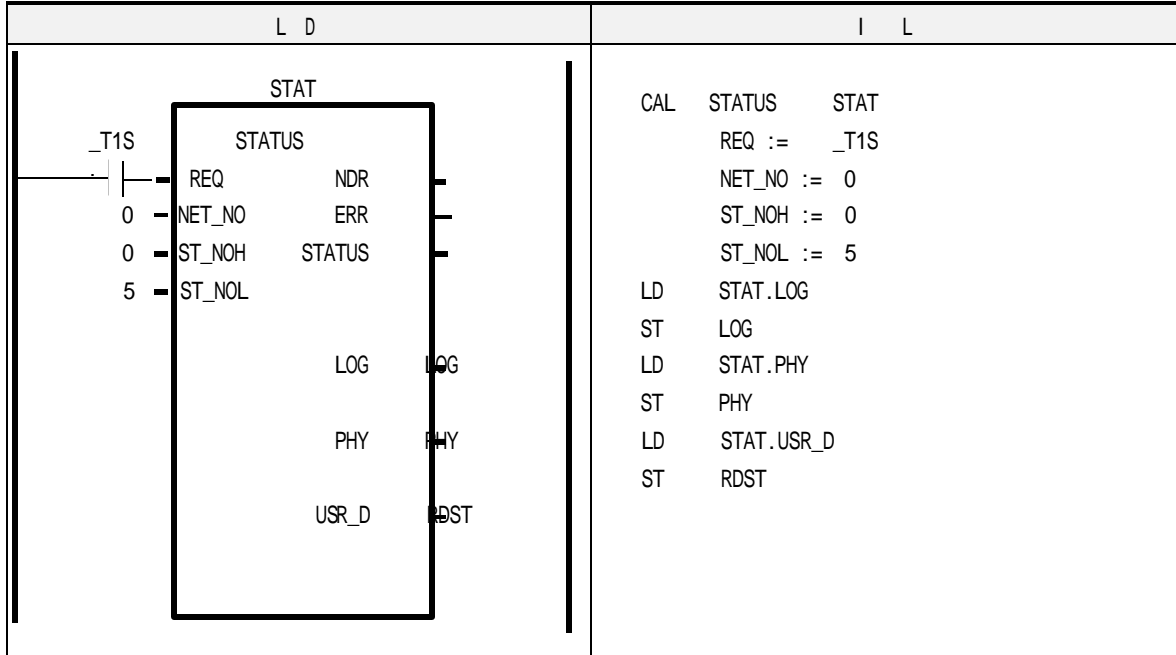
1 = PARTIALLY-OPERATIONAL-H/W(PLC 가 )

2 = INOPERABLE-H/W( )

3 = NEED-COMMISSION-H/W( )

v USR\_D  
 PLC  
 128

v : Fnet , 0 Fnet 가  
 5 128 RDST  
 (REQ 1 )





S[26]	_SYS_STATE	BIT 10		On/Off	
S[27]		BIT 11		ON/Off	
S[28]		BIT 12	ESTOP STOP	RUN	ESTOP
S[29]		BIT 13			
S[30]		BIT 14			
S[31]		BIT 15	ON		
S[32]	_PADT_CNF	BIT 0	GMWIN	GMWIN	
S[33]		BIT 1	GMWIN	GMWIN	
S[34]		BIT 2			
S[35]	_DOMAIN_ST	BIT 0			
S[36]		BIT 1	I/O	I/O	
S[37]		BIT 2			
S[38]		BIT 3			
S[39]		BIT 4			
S[40]	_CPU_ER	BIT 0	CPU	CPU 가 , CPU CPU 가 ( _SYS_ERR )	
S[41]	_IO_ER	BIT 1		I/O , ( _IO_TYER_N, _IO_TYER[n] )	
S[42]	_IO_TYER	BIT 2		, ( _IO_DEER_N, _IO_DEER[n] )	
S[43]	_FUSE_ER	BIT 3		가 ( _FUSE_ER_N, _FUSE_ER[n] )	

S[44]	_IO_RWER	BIT 4	/ ( ) (_IP_RWER_N, _IO_RWER[n])
S[45]	_SP_IFER	BIT 5	/ , 가 ( ) (_IP_IFER_N, _IP_IFER[n])
S[46]	_ANNUN_ER	BIT 6	_ANC_ERR[n],
S[47]			
S[48]	_WD_ER	BIT 8	SCAN WATCH-DOG (SCAN WATCH-DOG TIME)
S[49]	_CODE_ER	BIT 9	
S[50]	_STACK_ER	BIT 10	STACK OVERFLOW
S[51]	_P_BCK_ER	BIT 11	가 가 (_DOMAIN_ST )
S[52]	_RTC_ERR	BIT 0	( ) RTC RTC
S[53]	_D_BCK_ER	BIT 1	BACK_UP 가 , BACK_UP 가 , 가 .
S[54]	_H_BCK_ER	BIT 2	가 BACK_UP , ( ) 가 .

S[55]	_AB_SD_ER	BIT 3	(Abnormal Shutdown) 가 , 'ESTOP'
S[56]	_TASK_ERR	BIT 4	(TASK) 가 ( , _TC_BMAP[n],_TC_CNT[n] )
S[57]	_BAT_ERR	BIT 5	
S[58]	_ANNUN_WR	BIT 6	_ANC_WB[n] ,
S[59]			
S[60]			
S[61]	_HSPMT1_ER	BIT 8	1 가
S[62]	_HSPMT2_ER	BIT 9	2
S[63]	_HSPMT3_ER	BIT 10	3
S[64]	_HSPMT4_ER	BIT 11	4

## 6.5.7

가 On , STATUS

1)

(10 )	
0	( )
1	( , 가) : Off, , .
3	가 . :
4	
5	:
6	가 가 :
7	가 가 :
8	가 가 가
9	가 가 -
10	(Time Out) -
11	Structure
12	Abort( / ) :
13	Reject( / ) : MMS .
15	
33	:
34	: Structure (Range)
50	: CPU
113	Object Access Unsupported - VMD Specific Symbolic Address
187	( ) -

## 2) CPU STATUS

(1)

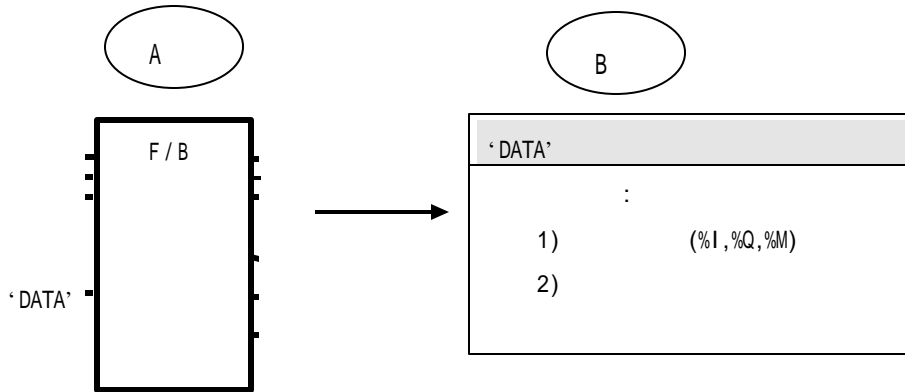
(10 )	
16	
17	SLOT_NO
18	
19	
20	
21	( -Time Out)

(2) (FSM) STATUS

(10 )	
128	FSM
129	BASE(Rack)
130	
131	
132	(Invalid Range)
133	
136	( )
137	

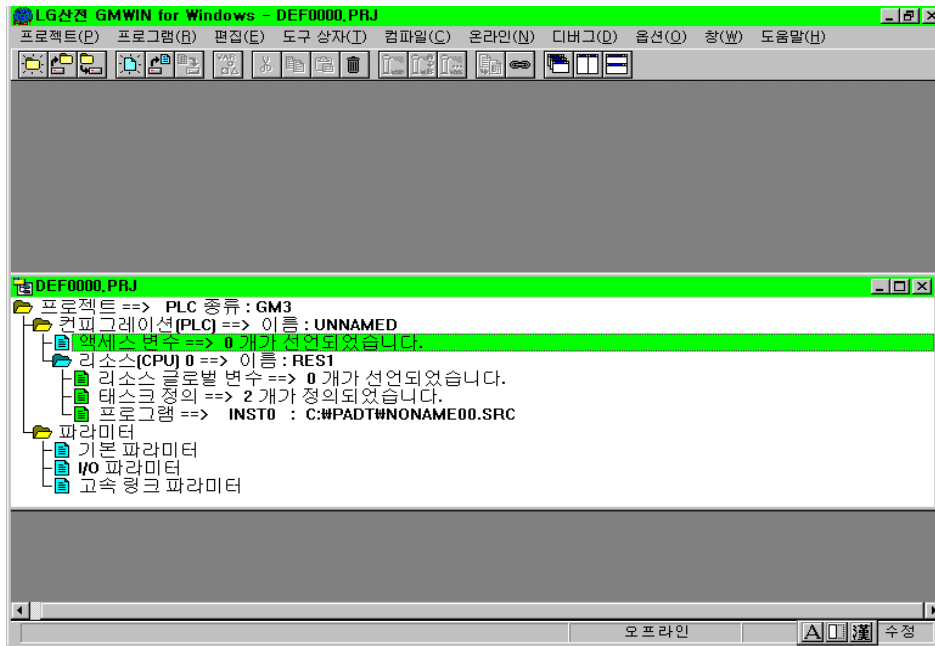


6.5.8



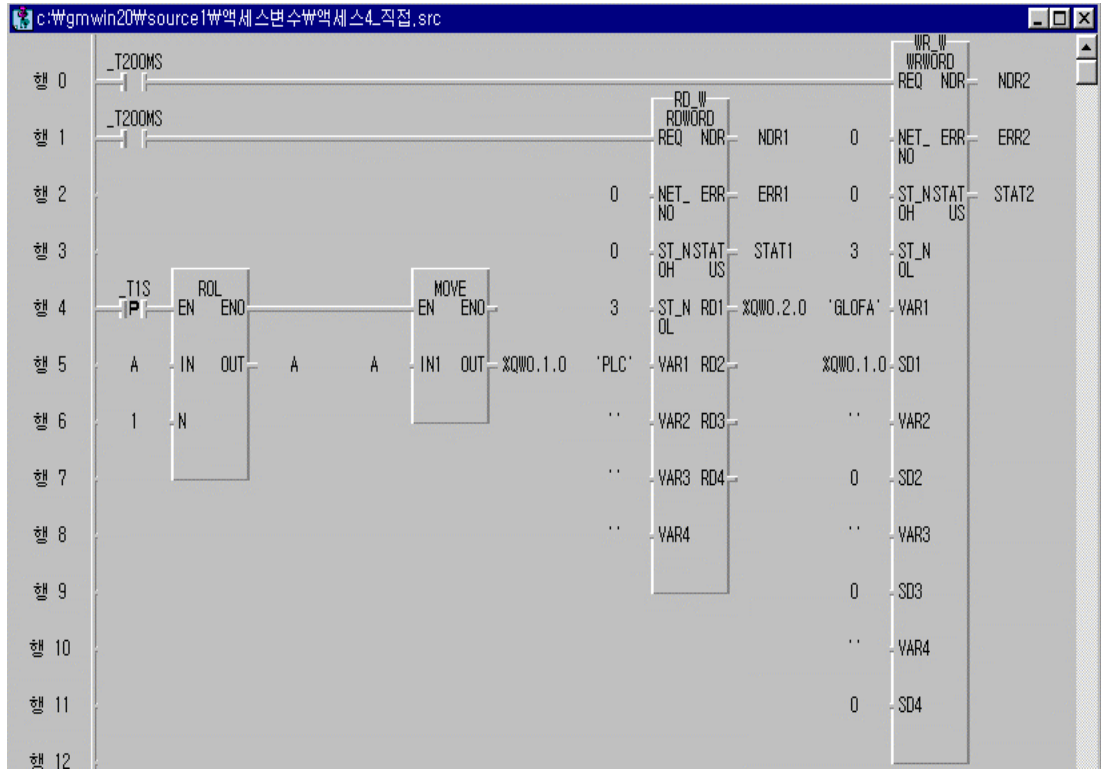
[ 6.4.8(A)]

(VAR1-4) ,  
 (M), (I), (Q)  
 BOOL, BYTE , WORD, DWORD, LWORD 가 .  
 가 가 ,  
 가 가 .  
 가 ' DATA ' 가  
 가 ' DATA ' 가  
 가 .

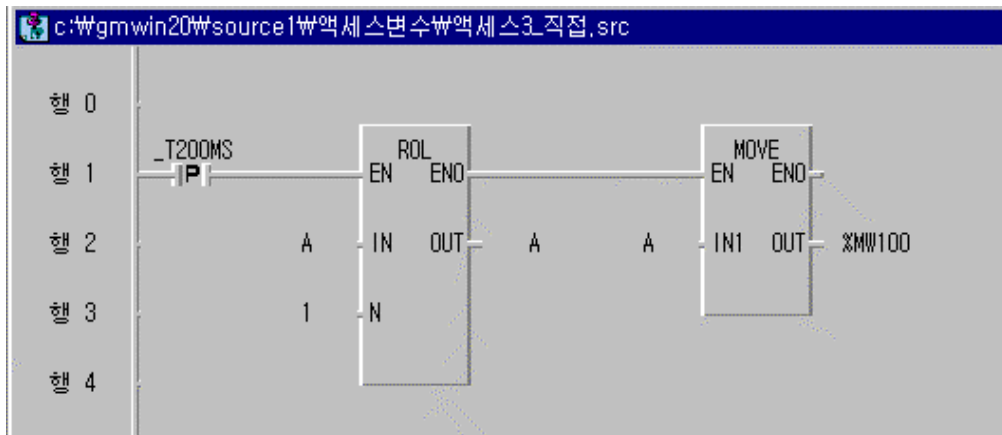


[ 6.4.8(B)]

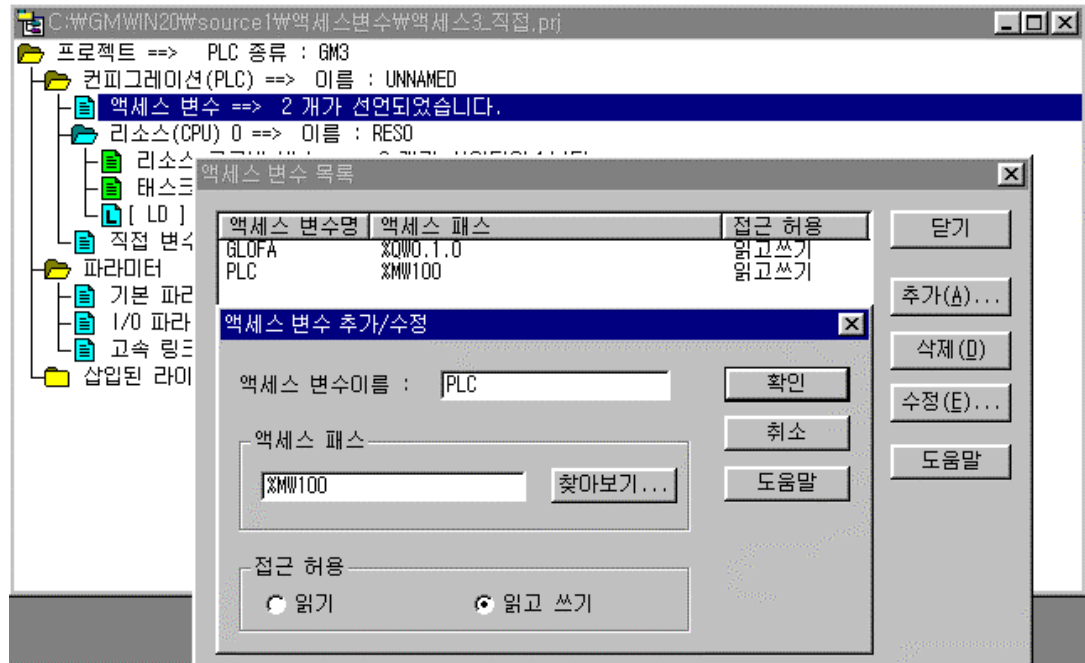
1) (%I, %Q, %M)\_



[ 6.4.8(C) ] A



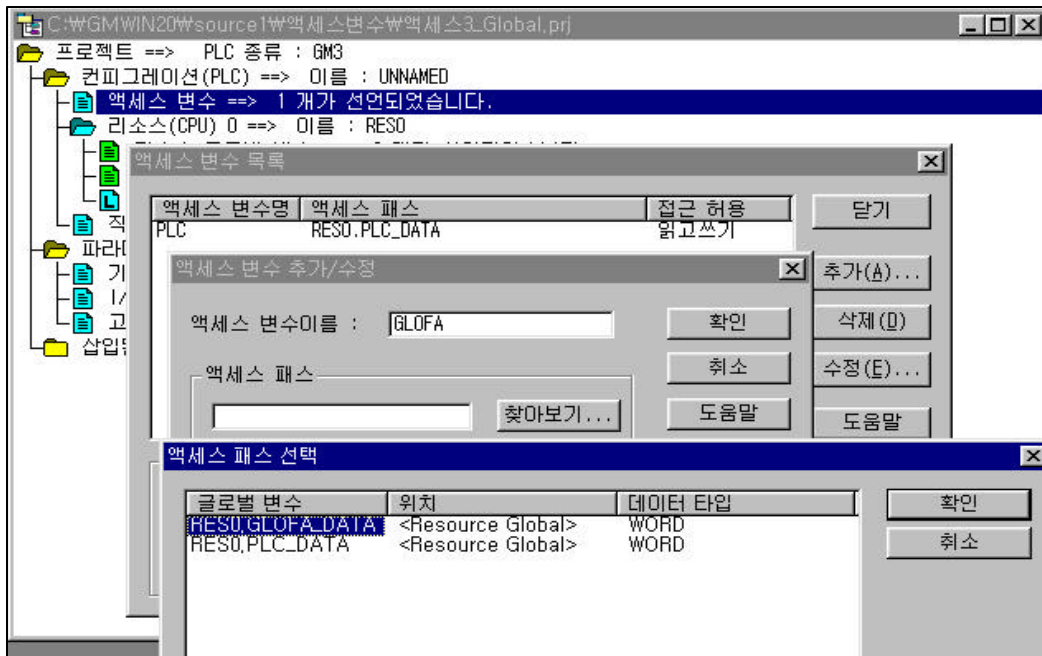
[ 6.4.8(D) ] B



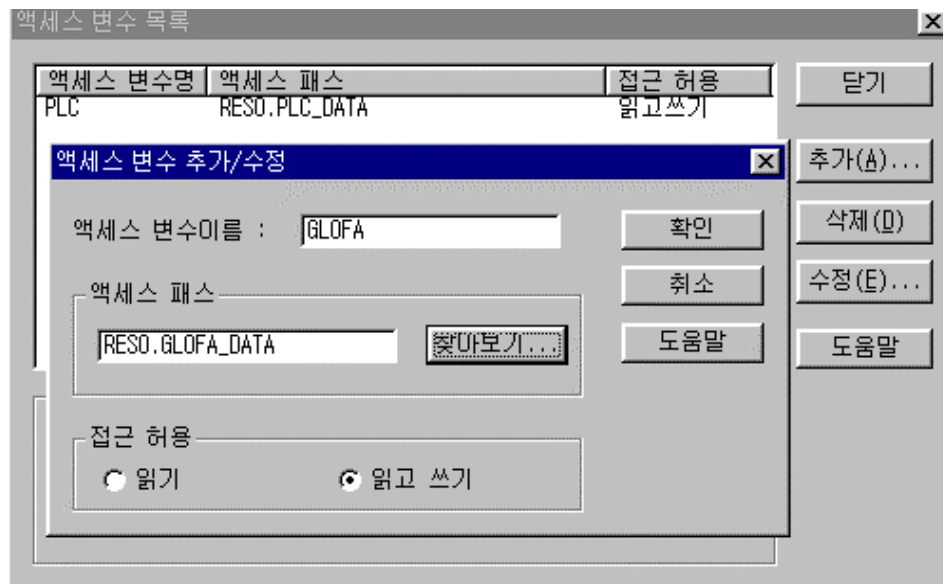
[ 6.4.8(E)]

A B ' PLC ' ' GLOFA ' B  
 ' PLC ' ' GLOFA 가  
 [ 3.8(E)] 가/ PLC  
 ( 가/  
 VAR1 - 4, VAR 가 가  
 ), %MW100 PLC %MW100  
 A B ' PLC ' B %MW100  
 가 GLOFA ( )





[ 6.4.8(G) ]



[ 6.4.8(H) ]

[ 6.4.8(H)]

‘ RES0 ’

GM1, GM2 128 , GM3, GM4, GM5, GM6 64

가

RES0.PLC\_DATA

RES0

(GM1

4

CPU

RES0,1,2,3

가

GM1 CPU 4

GM2, GM3,

GM4, GM5, GM6

RES0

)

RES0

)

6.7

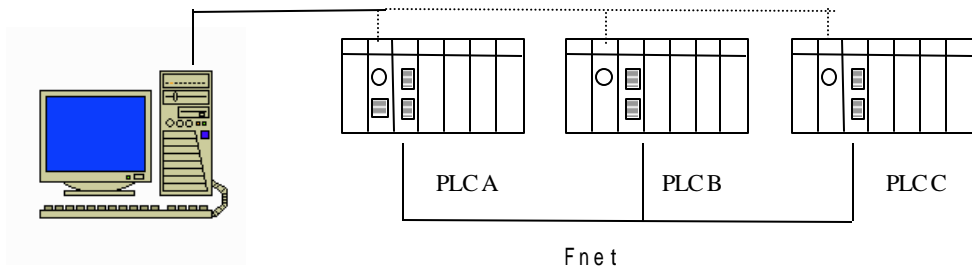
6.7.1

PLC 가 Fnet

(GMWIN/KGL-WIN)

가

가

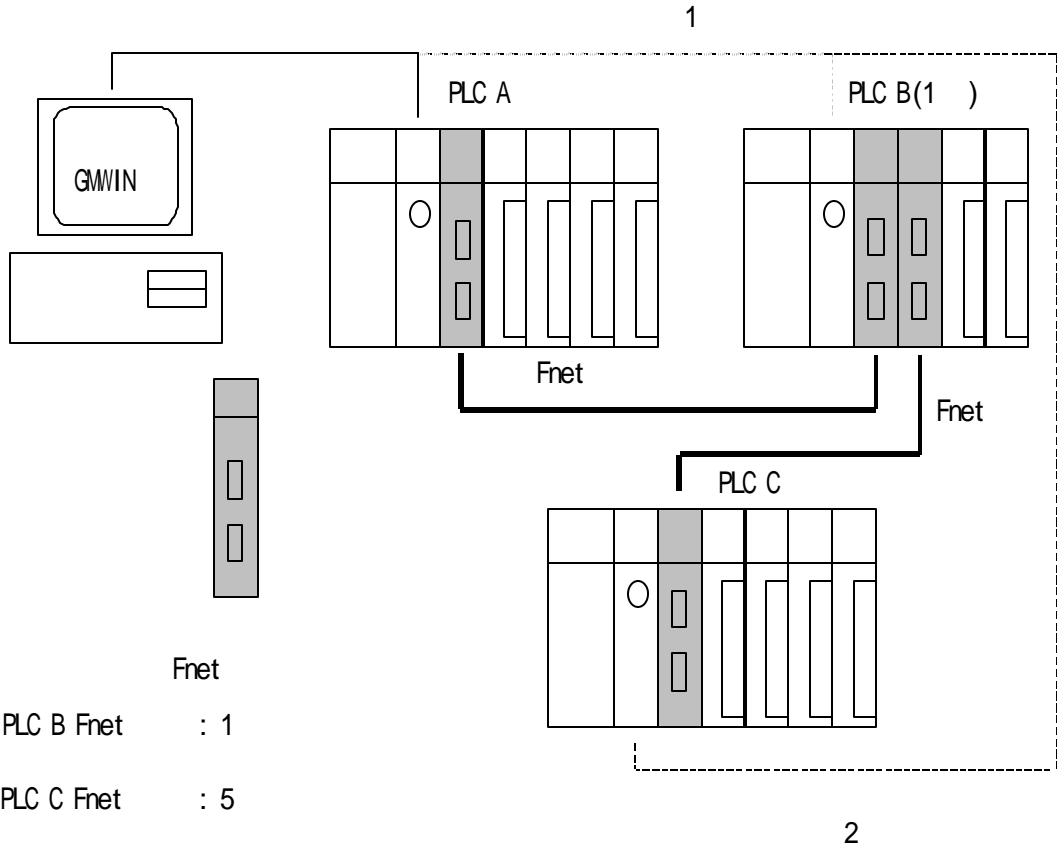


[ 6.6.1 ]

(GMWIN/KGL-WIN) RS-232C PLC A CPU  
 PLC A, PLC B PLC C 가 Fnet 가  
 PLC C 1 / 2  
 PLC C ( ), PLC A ( )  
 PLC A ) RS-232C Fnet  
 RS-232C PLC C  
 PLC A  
 PLC  
 가 PLC

6.7.2 GMWIN

GLOFA Fnet PLC 1 2  
 ( , GM7-Fnet 1 가 .)

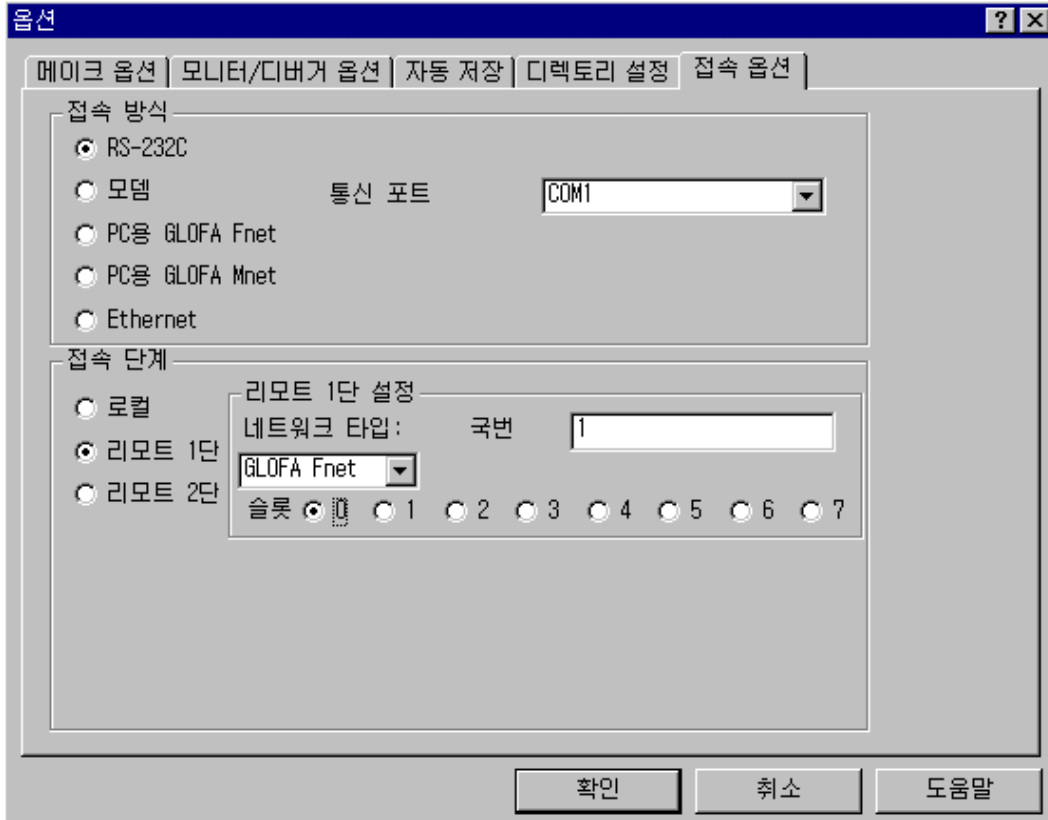


[ 6.6.2] 1 / 2

[ 6.6.2] 1 (PLC A ,PLC B) 2 (PLC C)



1 : 1 GMWIN (P)→ (Q)...→ 1



: 1 . [ 6.6.2]

1 Fnet GLOFA Fnet

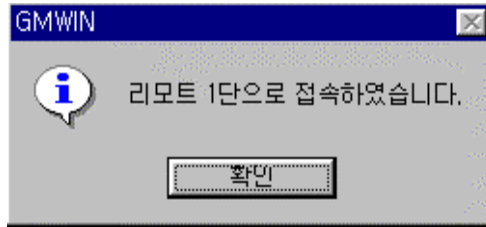
: 1 PLC ([ 6.6.2]

PLC B 1)

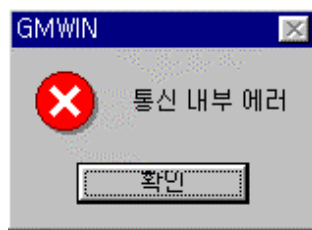
: 1 PLC

→

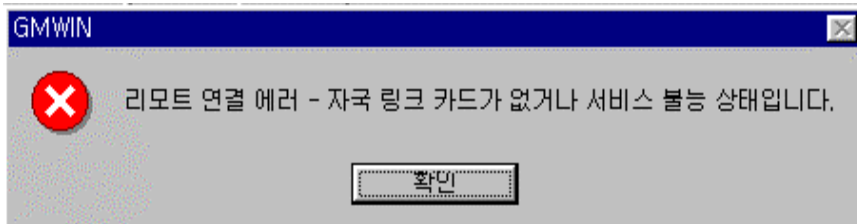
1 가 ,



, 가 .

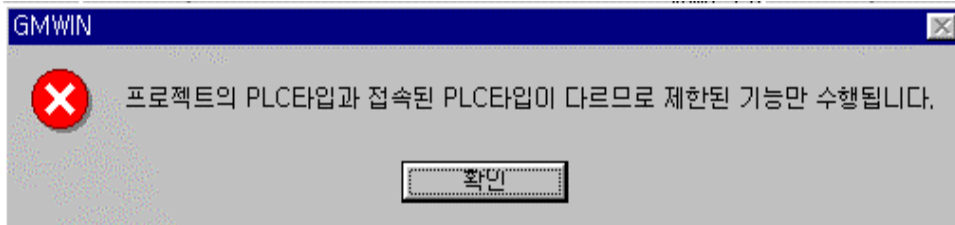


( / )

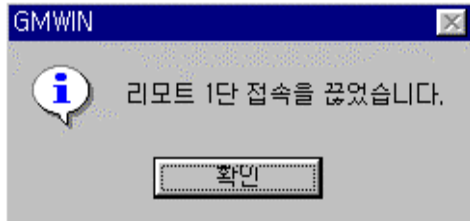


( )

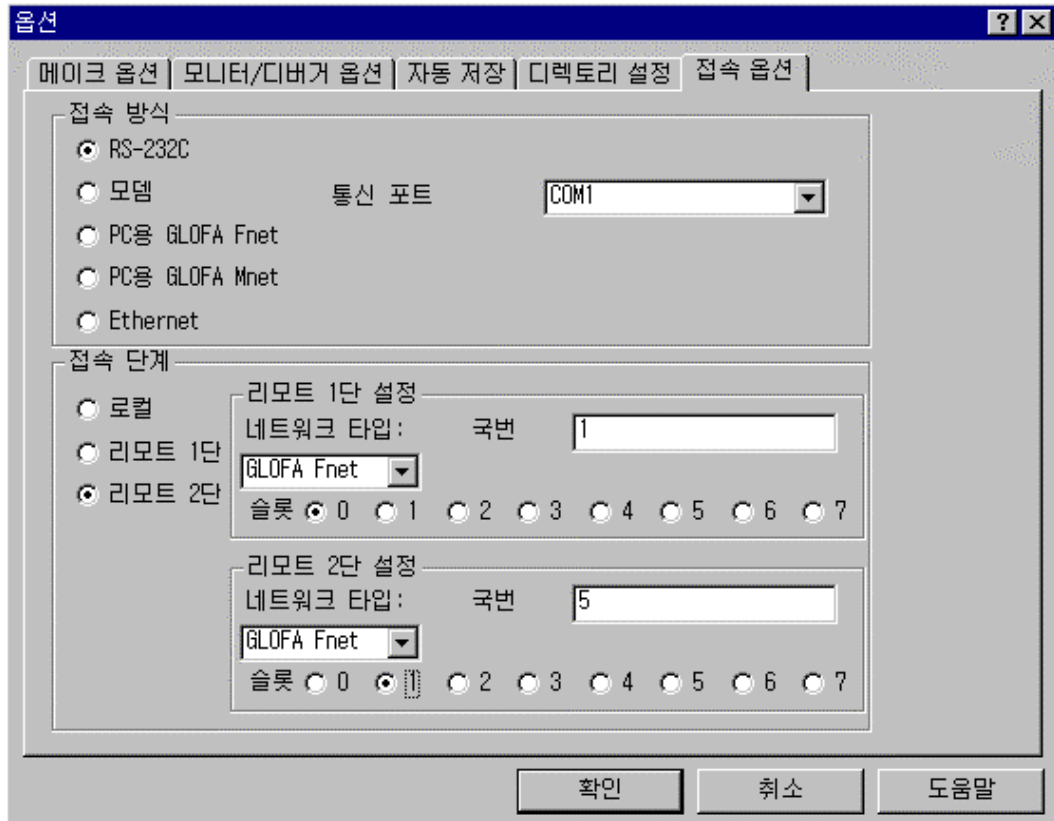
1 PLC CPU 가



1 RS-232C ( PLC CPU 가 ) . 1



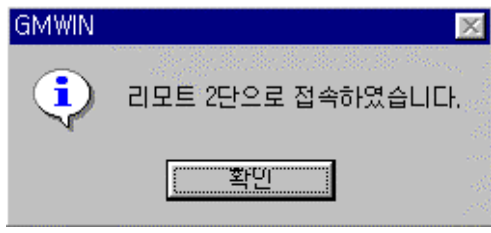
2 : 2 GMWIN PLC A Fnet PLC B Fnet(0 ) PLC B  
 Fnet(1 ) PLC C Fnet 2  
 2 GMWIN  
 (P) → (Q) ... →  
 2  
 .( , GM7-Fnet 1 )



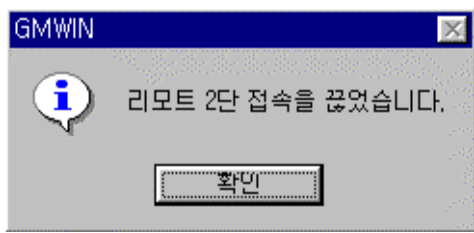
: 1 2 . 1  
 2  
 [ 6.6.2] 1 2 GLOFA Fnet

: 1 2  
 1 PLC B 1 , 2 PLC C 5  
 16 16#?????  
 16# 10

: 1 PLC A PLC B PLC A  
 0 , PLC B PLC C 2 PLC B  
 1  
 2 가



2 , PLC C RS-232C  
 가

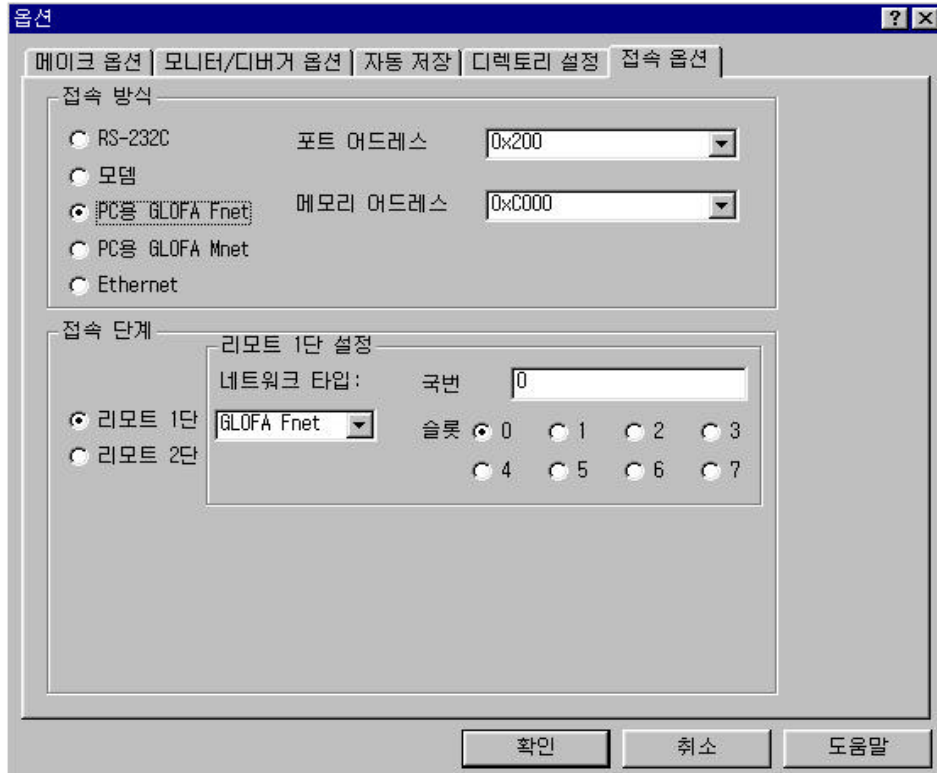


GMWIN RS-232C ( )  
 ( ) 가

[ 6.6.2] GMWIN

	PC- (GMWIN)	GM1	GM2	GM3	GM4	GM6	GM7	GM3 I/O	GM4 I/O
PC- (GMWIN)	X	0	0	0	0	0	0	0	0
GM1	X	0	0	0	0	0	0	0	0
GM2	X	0	0	0	0	0	0	0	0
GM3	X	0	0	0	0	0	0	0	0
GM4	X	0	0	0	0	0	0	0	0
GM6	X	0	0	0	0	0	0	0	0
GM7	X	0	0	0	0	0	0	0	0
GM3 I/O	X	0	0	0	0	0	0	0	0
GM4 I/O	X	X	X	X	X	X	X	X	X

GM3 I/O(G3L-RBEA) RS-232C 가  
 GM3 I/O GM1 ~ GM7 PLC GMWIN  
 (GM4,GM6,GM7 )  
 PC (GOL-FUEA) GMWIN GMWIN



PC

GMWIN 1 2

1) GMWIN , 1 2 CPU

- (1)
- (2)
- (3)
- (4)
- (5)
- (6) I/O
- (7) I/O
- (8) I/O SKIP

2) GMWIN 1 2

3) GM3/GM4 I/O

- (1)
- (2)
- (3)
- \*
- \*
- \*
- \* I/O
- \*
- \*
- \*
- \*
- (4)
- (5)
- (6) I/O SKIP

4) 2

5) GM7-Fnet 1

가

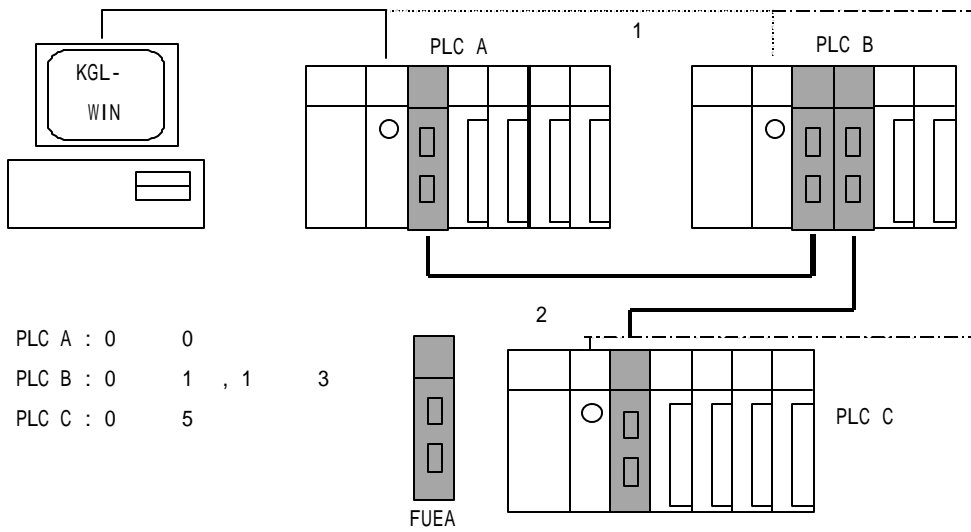




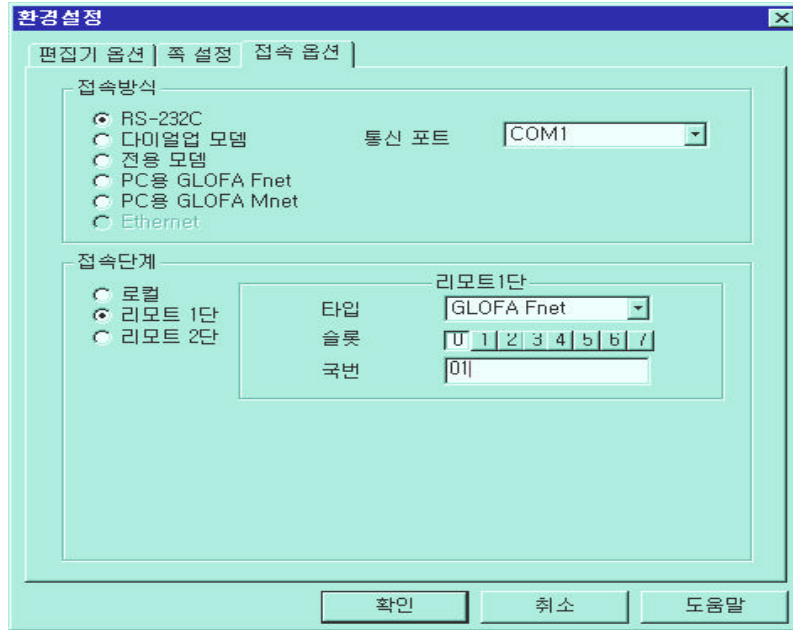
6.7.4 KGL-WIN

MK PLC(K1000S I/O K300S/K200S I/O )  
 KGL-WIN 가 . KGL-WIN 1 , 2  
 . 1 2 . [ 6.6.4]  
 1 (PLC A, PLC B) 2 (PLC C) .

[ 6.6.4] KGL-WIN ( 1 , 2 )

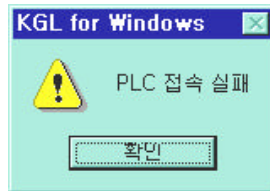


(가) 1 : 1 KGL-WIN



: RS-232C .  
: 1 , Fnet .  
: PLC .  
[ 6.6.4] 0 .  
: 1 PLC , [ 6.6.4]  
PLC B h01 . 10 h 10 1

1 KGL-WIN PLC 가  
가 .





: 1 PLC A PLC B PLC A  
 0 , 2 PLC B PLC C 2  
 PLC B 1 .

: 1 2 .  
 1 PLC B 1 , 2 PLC C 5 .  
 , KGL-WIN OK  
 , 가  
 2 , PLC C RS-232C

6.6.1] KGL-WIN RS-232C  
 ( ) Fnet  
 ( ) 가

[ 6.6.1]KGL-WIN

	PC- (KGL-WIN)	K1000S	K300S	K200S	K1000S K300S	
					I/O	I/O
PC- (KGL-WIN)	X	0	0	0	0	0
K1000S	X	0	0	0	0	0
K300S	X	0	0	0	0	0
K200S	X	0	0	0	0	0
K1000S I/O	X	0	0	0	0	0
K300S I/O	X	X	X	X	X	X

K1000S RS-232C 가 K1000S K1000S ~  
 K200S PLC KGL-WIN  
 ( K300S/K200S )

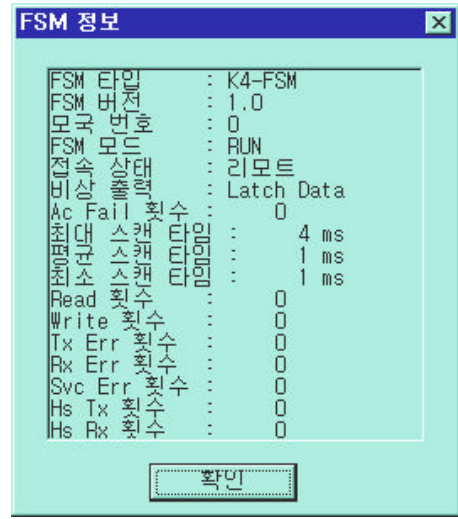
- KGL-WIN 1 2
- 1) KGL-WIN , 1 2 CPU
  - 2) KGL-WIN 1 2
  - 3) 2 가

6.7.5 KGL-WIN I/O

KGL-WIN I/O I/O

KGL-WIN I/O 가  
 \* (PLC)  
 \* I/O  
 \*  
 \*  
 \* (P )

(가) (PLC)  
 I/O  
 PLC



FSM ⇒ I/O

FSM ⇒ I/O O/S

⇒ I/O PLC

FSM ⇒ I/O (RUN/ STOP)

RUN :

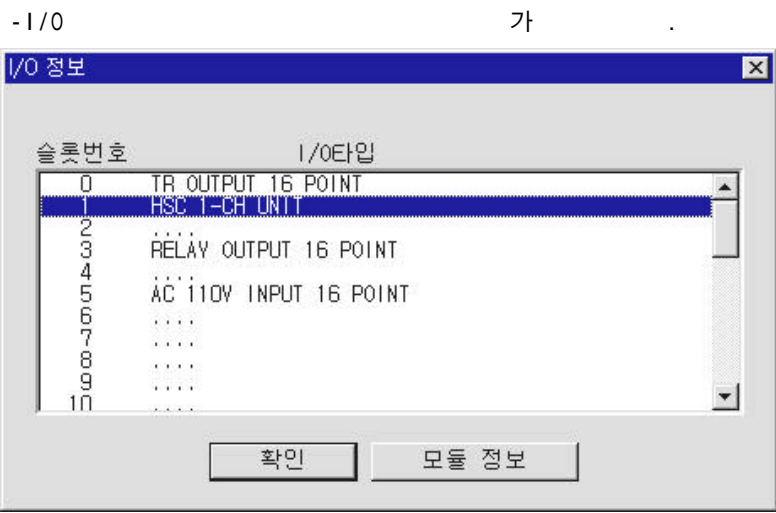
STOP : /

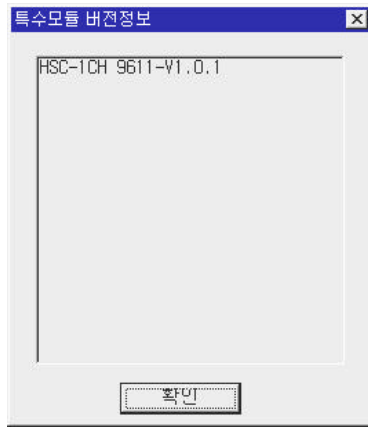
```

⇒ KGL-WIN          I/O
  Remote :          I/O      KGL-WIN
  Local  :          I/O
⇒
  Data Latch :
:
AC Fail ⇒
⇒ (Token)
⇒ (Token)
⇒ (Token)
Read ⇒ Read          Read
Write ⇒ Write        Write
Tx Err ⇒ ( )
, 가
가 가 가
Rx Err ⇒ ( )
Svc Err Count ⇒ NAK
HS Tx Count ⇒ 가
HS Rx Count ⇒ 가

```

( ) I/O  
I/O FSM





( )

가

( ) P

P

/

P

( ) K1000S/K300S/K200S I/O

1)

2)

3)

\*

\*

\*

\*

I/O

\*

\*

\*

\*

4)

5) Fnet , Fnet

6.7.6

FSM

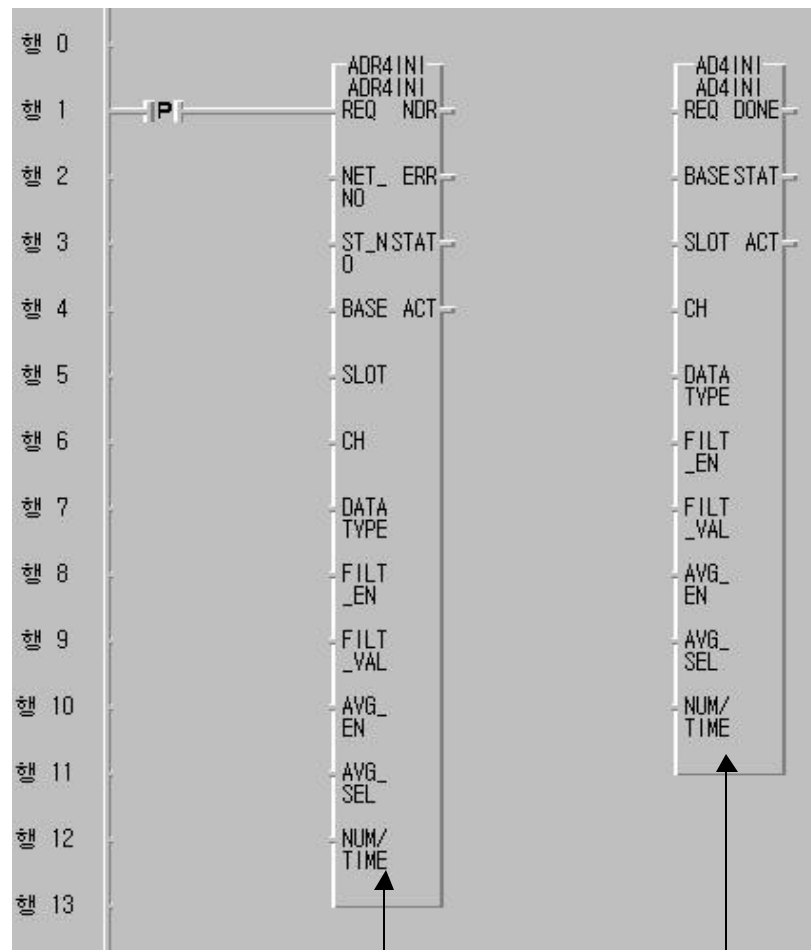
가 가





6.8.1 GMWIN

GLOFA Fnet  
 가 D/A , A/D ,  
 가 8 [ 8.1.2]  
 NET\_NO, ST\_NO,  
 ERR, NDR 가 [ 6.8.1(A)] A/D  
 CPU AD AD



(A)

(B) CPU

[ 6.8.1(A)] AD

[ 6.8.1(A)] CPU CPU

가

[ 6.8.1(A)] 가

[ 6.8.1(A)]

REQ ( )	'0' '1'	(Bool)
NET_NO ( )	PLC	0 ~ 7
ST_NO ( )	,	0 ~ 63
NDR ( )	On	On/Off
ERR ( )	가 On.	On/Off
BASE ( )	,	0 ~ 3
SLOT ( )	,	0 ~ 7

[ 6.8.1(A)]

[ 6.8.1(B)]

CPU		GM1, GM2	GM3	GM4	GM6	GM7	
ADRxINI (x= 2,4)	ADR2INI	X	X	0	X	X	4
	ADR4INI	0	0	X	X	X	16
ADRxRD (x= 2,4)	ADR2RD	X	X	0	X	X	4
	ADR4RD	0	0	X	X	X	16
DARxINI (x= 1,4)	DAR1INI	X	X	0	X	X	2
	DAR4INI	0	0	X	X	X	16
DARxWR (x= 1,2,4)	DAR1WR	X	X	0	X	X	2
	DAR2WR	X	X	X	X	X	4
	DAR4WR	0	0	X	X	X	16
HSCRx_RD (x= 0,1)	HSCR0RD	X	X	0	X	X	1
	HSCR1RD	0	0	X	X	X	2
HSCRx_SET (x= 0,1)	HSCROSET	X	X	0	X	X	1
	HSCR1SET	0	0	X	X	X	2
HSCRx_WR (x= 0,1)	HSCROWR	X	X	0	X	X	1
	HSCR1WR	0	0	X	X	X	2
RTDxINI (x= 2,3)	RTDR2INI	X	X	0	X	X	4
	RTDR3INI	0	0	X	X	X	8
RTDxRD (x= 2,3)	RTDR2RD	X	X	0	X	X	4
	RTDR3RD	0	0	X	X	X	8
TCRxINI (x= 2,4)	TCR2INI	X	X	0	X	X	4
	TCR4INI	0	0	X	X	X	16
TCRxRD (x= 2,4)	TCR2RD	X	X	0	X	X	4
	TCR4RD	0	0	X	X	X	16

1) CPU

CPU

2)

ADRxINI, ADRxRD

'R' (

)

, x

2 x

6.8.2 KGL - WIN

MASTER-K KGL-WIN  
'RGET' , 'RGET'  
, '6-6 MASTER-K '

6.9

GLOFA GMWIN , CPU Fnet  
 , MASTER-K KGL-WIN

6.9.1

1)

(1) \_NETx\_LIV[n] ([n]: , n = 0~63, x: )  
 Alive ,  
 가 ,

(2) \_NETx\_RST[n]

'On'

2)

I/O

I/O,

가

(1) \_FSMx\_RESET

FSM

FSMx\_ST\_NO

, \_FSMx\_RESET

'On'

, 'On'

(2) \_FSMx\_IO\_RESET

FSM

가

\_FSMx\_ST\_NO

, \_FSMx\_IO\_RESET

'On'

'On'

3)

(1) \_FSMx\_HS\_RESET

( , ) 가  
 On \_HS\_MODE  
 Off ( ).  
 \_HS\_MODE 가 (On)가  
 FSMx\_HS\_RESET On \_HS\_MODE  
 \_FSMx\_ST\_NO , \_FSMx\_HS\_RESET 'On' \_HS\_MODE '1'

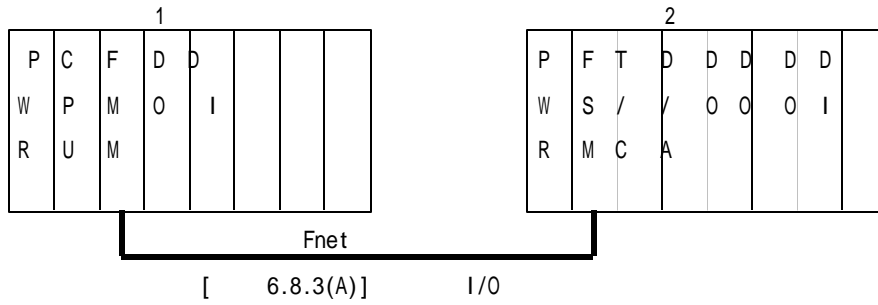
4)

\_FSMx\_RESET/\_FSMx\_IO\_RESET/\_FSMx\_HS\_RESET  
 255(16#FF)  
 \_FSMx\_RESET/\_FSMx\_IO\_RESET/\_FSMx\_HS\_RESET

6.9.2 Fnet

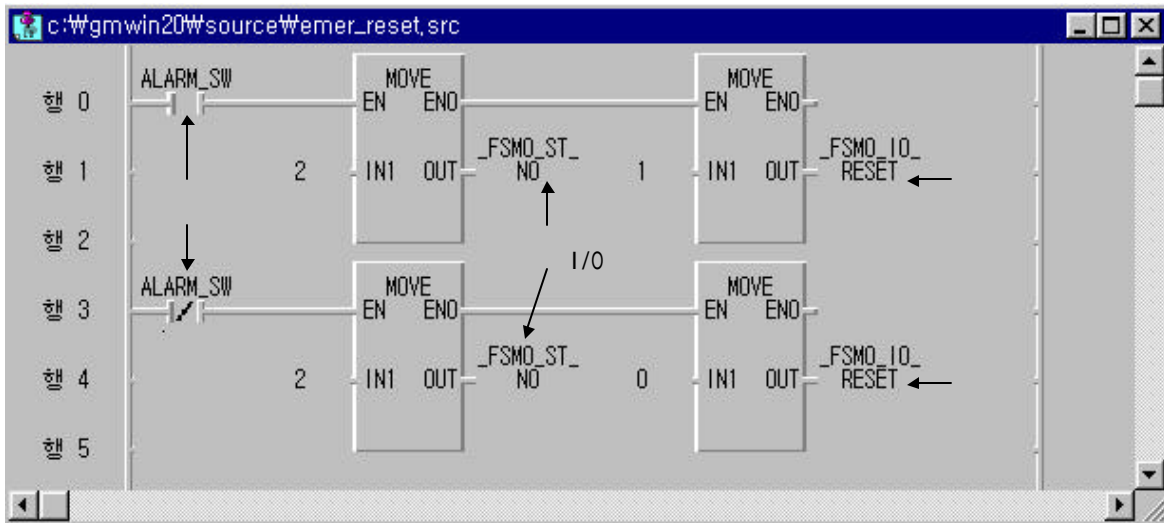
_FSMx_ST_NO 0 ~ 63 (255 )	USINT	/ 가	FSM
_FSMx_RESET	BOOL	/ 가	
_FSMx_IO_RESET	BOOL	/ 가	
_FSMx_HS_RESET	BOOL	/ 가	
_NETx_LIV[n] ( n = 0 ~ 8)	USINT		FSM/FMM
_NETx_RST[n] ( n = 0 ~ 63)	USINT	/ 가	

6.9.3 I/O ( \_FSMx\_RESET / \_FSMx\_IO\_RESET )



[ 6.8.3(A) ] PLC CPU FMM, FSM I/O

1) \_FSMx\_IO\_RESET (GMWIN)  
 PLC CPU I/O  
 [ 6.8.3(B) ]



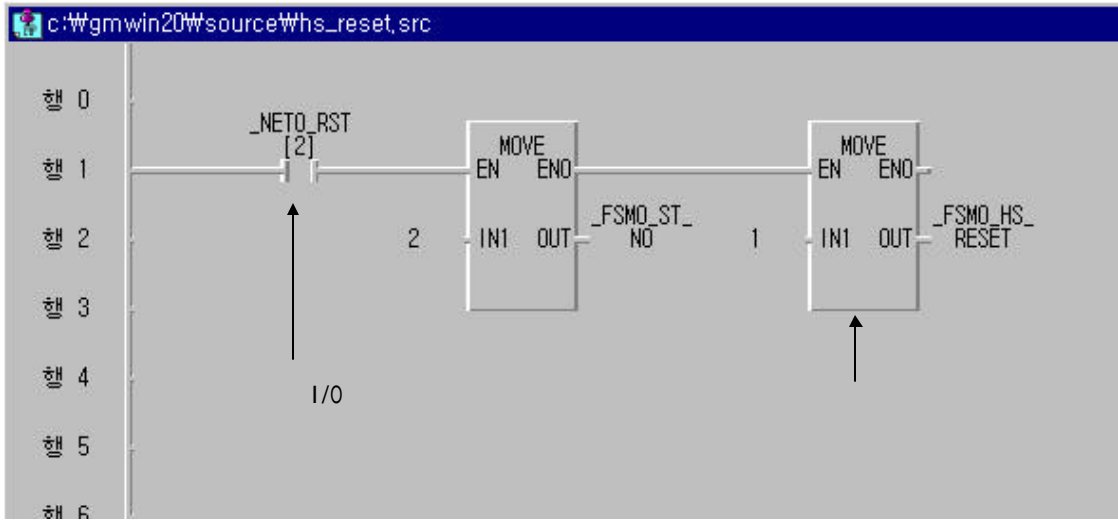
[ 6.8.3(B) ] I/O

I/O ALARM\_SW  
 가 '0n' '\_FSMO\_ST\_NO' I/O 2  
 '\_FSMO\_IO\_RESET' '1' I/O , '\_FSMO\_ST\_NO'  
 '\_FSMO\_IO\_RESET' '0' FMM , '\_FSMO\_ST\_NO' FSM  
 '\_FSMO\_IO\_RESET' '1' I/O  
 '\_FSMO\_IO\_RESET' '0' I/O





6.9.4



[ 6.8.4(A)] \_FSMx\_HS\_RESET

[ 6.8.4(A)] [ 6.8.3(A)] I/O

. \_NETO\_RST[2]

0 2 ( ) 2

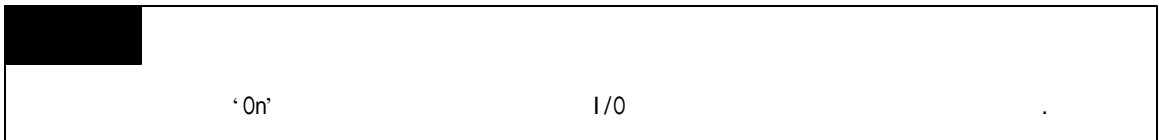
On . \_HS\_MODE

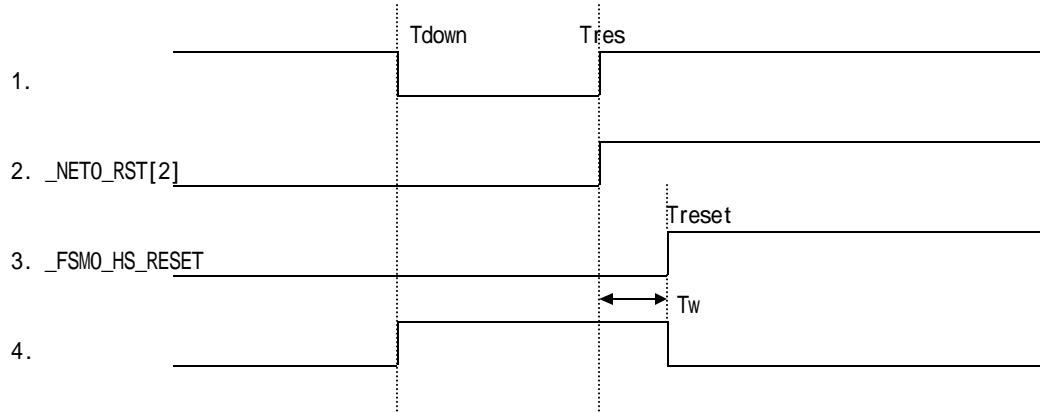
가 '0' '1'

\_FSMO\_ST\_NO \_FSMO\_HS\_RESET '1' \_HS\_MODE

'1' '1'

I/O ,





[ 6.8.4(B) I/O

[ 6.8.4(B) Tdown '0n' Tres 가  
 \_FSMO\_HS\_RESET Treset '1' Tw  
 '1'

6.9.5 ( \_NETx\_LIV[n], \_NETx\_RST[n] )

[ 6.8.3(A) \_NETx\_LIV[n], \_NETx\_RST[n] I/O

I/O CPU

1)

가

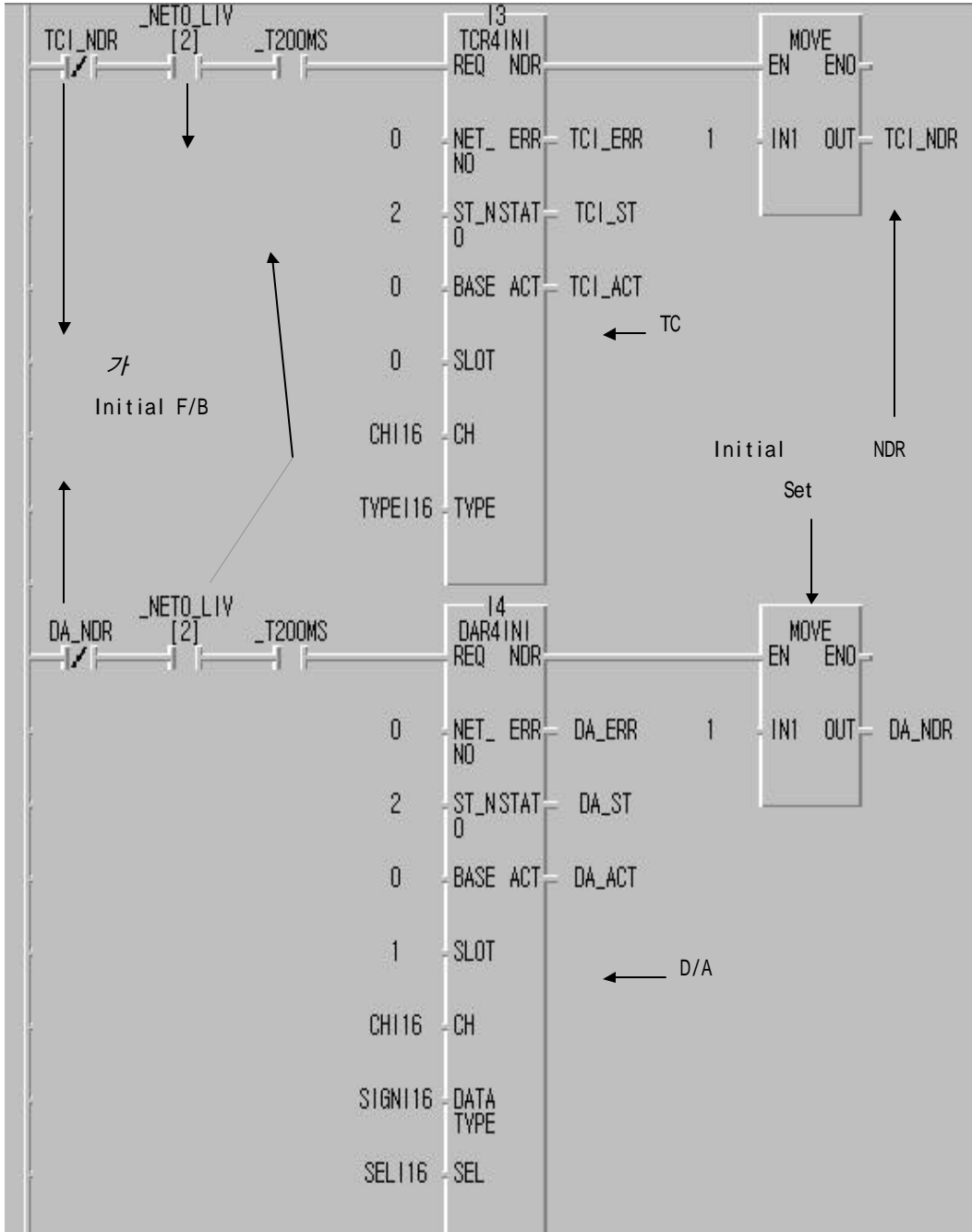
2)

3) Request

4)

/

가 가

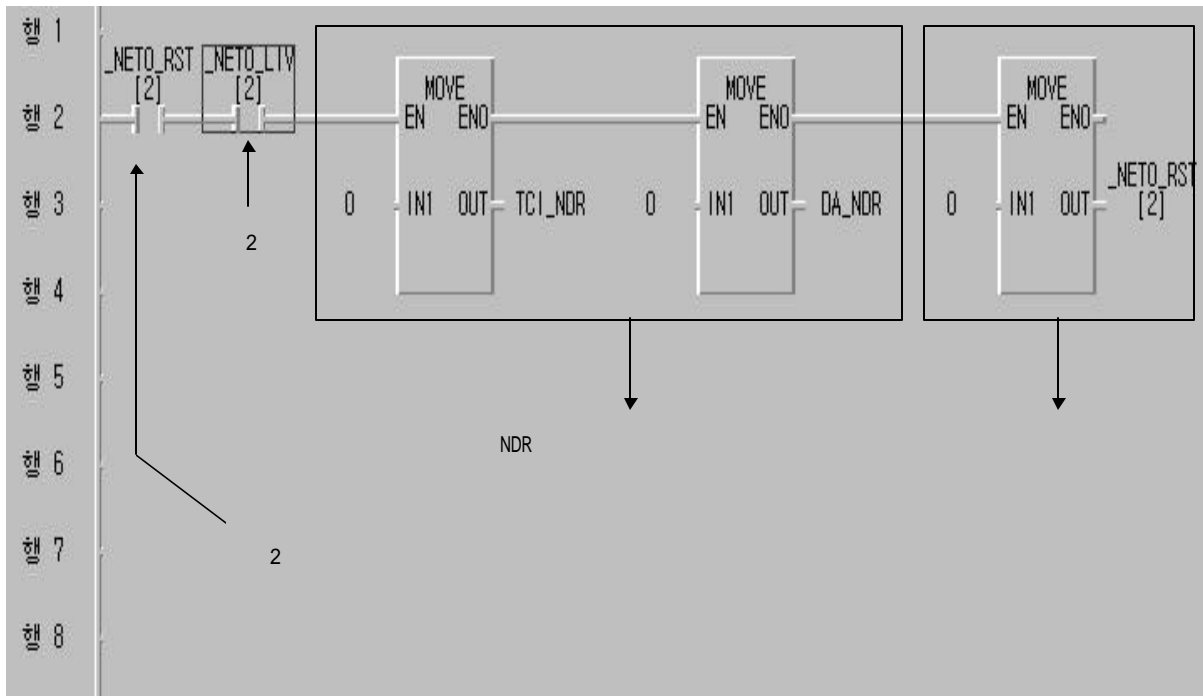


[ 6.8.5(A) I/O (GMWIN )

[ 6.8.5(A) [ 6.8.3(A) 0,1 T/C, D/A

F/B NDR B Request  
가 200 ms

가 NDR B  
 Request  
 \_NETO\_LIV[2] 0 FMM 2  
 . \_NETO\_LIV[2]  
 / Request  
 [ 6.8.5(B) I/O [ 6.8.5(A)



[ 6.8.5(B) (GMWIN )

[ 6.8.5(B) \_NETO\_RST[2] \_NETO\_LIV[2]  
 , NDR [ 6.8.5(B)  
 6.8.5(A) , \_NETO\_RST[2]  
 가 [ 6.8.5(B)  
 가 ,

6.9.6

(3~7 ) , Off  
 . (Fnet )

1) 가  
( ) .

2) 가 I/O  
2가 가 .

(1) GMWIN KGL-WIN  
OFF,ON 가

(2) OFF,ON 가

3) GLOFA GMWIN  
GMWIN I/O 1 /2  
(6.4.2 GMWIN ) .  
[ 6.8.5(B)] 가  
가 .



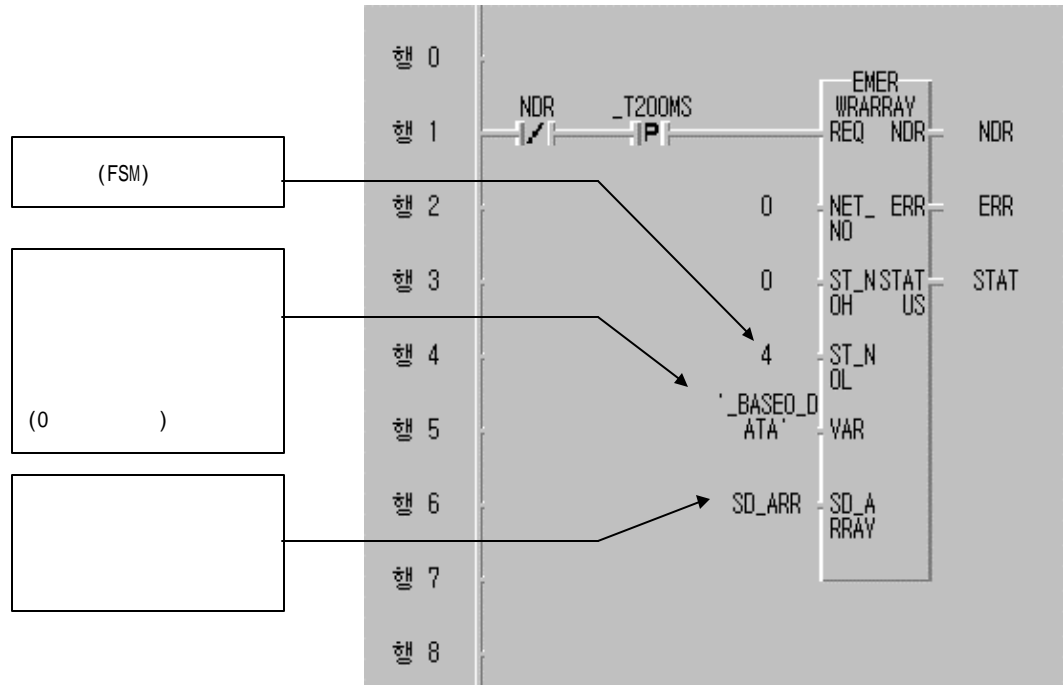
[ 6.8.5(A) ]



[ 6.8.5(B) ]

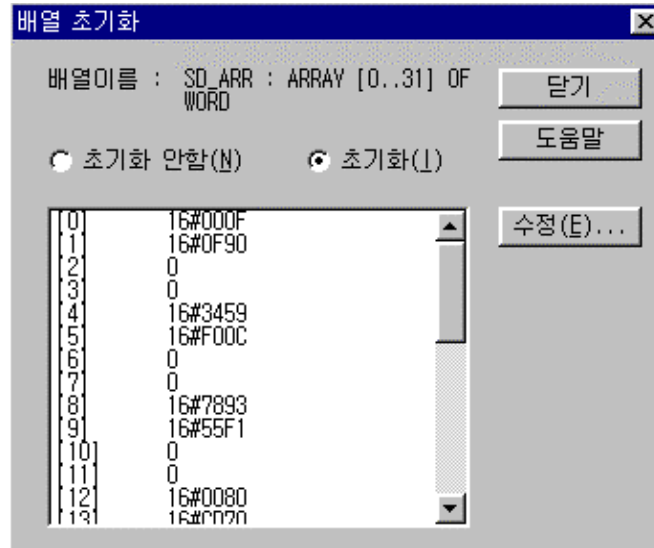




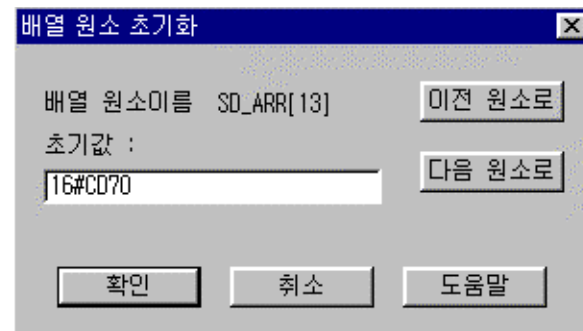


[ 6.8.5(D)] \_BASEx\_DATA





[ 6.8.5(F)]

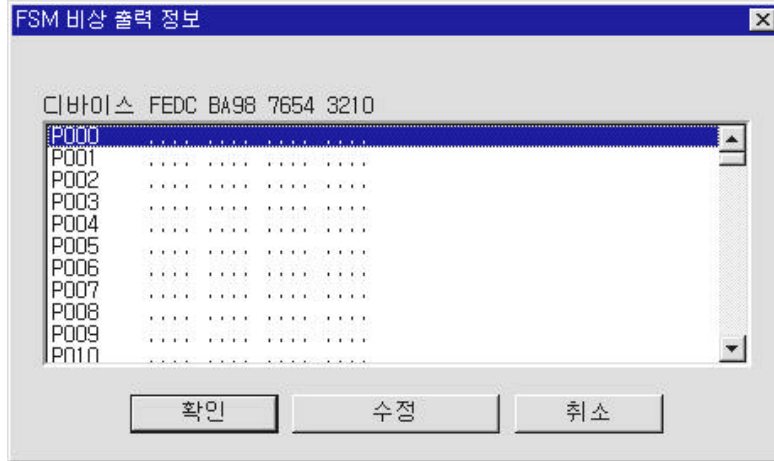


[ 6.8.5(G)]

5) MASTER-K KGL-WIN

KGL-WIN

P 가



[ 6.8.5(H) ] P

[ 6.8.5(H) ]



ON

On/Off

KGL-WIN

가 )

On/Off

, KGL-WIN

7.1 LED

7.1.1

LED

가

A/S

7.1.2 Fnet

LED

1) : G3L-FUEA/FUOA, G4L-FUEA/FUOA, G6L-FUEA, G0L-FUEA



G7L-FUEA



2) LED

(1) RUN : PLC CPU

가

- On : PLC

- Off :

' On '

PLC (Scan)

가

PLC

(200ms ) , PLC 2

' On ' 1,2

' On '

' Off '

가

(2) LAS : (Token)

- LED가 On .
- 가 LAS 가 ,
- LAS LED가 .
- On : Active Scheduler(LAS) .
- Off : (LM) .

(3) TOKEN : (Token) LAS

- . .
- On : (Token) .
- Off : (Token) .

(4) TX/RX :

- On : .
- Off : (Frame) .

(5) FAULT(ERR) :

- LED 'Off'
- 가 1
- , LED 0(RUN) ~ LED 4(Fault) 5 LED .

(6) LINK-I/F : Interface LED Fnet PLC CPU .

- Disable 2 .
- PLC CPU LINK 가 2

가

?

?

? ( )

?

750m ?

?

[ 7.1.2]. Fnet

LED

		LED	
FMM_00	ON	● ○ ○ ○ ○	1
FMM_01		○ ● ○ ○ ○	2
FMM_02		○ ○ ● ○ ○	
FMM_03		○ ○ ○ ● ○	CPU
FMM_04		● ○ ● ● ○	LAS 가
FMM_05		● ● ● ● ○	LAS
FMM_06		● ○ ○ ○ ○	1
FMM_07		○ ○ ○ ● ○	2
FMM_08		○ ○ ● ● ○	
FMM_09		○ ○ ● ● ●	
FMM_10		○ ● ○ ○ ○	RAM
FMM_11		○ ● ○ ● ○	CPU 1
FMM_12		○ ● ● ○ ○	CPU 2
FMM_13	○ ● ● ● ○	CPU 3	
FMM_14		● ○ ○ ○ ○	
FMM_15		● ○ ○ ● ○	
FMM_16		● ● ○ ○ ○	
FMM_17		● ● ○ ○ ○	,
FMM_18		● ● ● ● ○	/
FMM_19		● ● ○ ○ ○	
FMM_20		● ○ ● ● ○	
FMM_21		● ○ ○ ○ ○	
FMM_22			○ ● ● ○ ○
FMM_23	○ ○ ● ● ○		( ) LAS 가
FMM_24		● ● ● ● ●	
FMM_25		● ○ ○ ○ ○	
FMM_26		○ ○ ○ ○ ○	
FMM_27		○ ○ ○ ○ ●	

LED                      RUN, LAS, TOKEN, TX/RX, FAULT  
 ● ,                      ○ , 1                      ● ,                      off ○





(3) TX/RX :

- On :

- Off: (Frame)

(4) FAULT

- :

- Off :

가

?

?

? ( )

?

750m

?

?

(5) SYS FAULT :

LED

' Off '

가

1

LED 0 ~ LED 4 5

LED

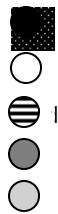
[ 7.1.3].

LED

		LED	
FSM_00	On	● ○ ○ ○ ○	1
FSM_01		○ ■ ○ ○ ○	2
FSM_02		○ ○ ■ ○ ○	
FSM_03		○ ○ ○ ● ○	
FSM_04		● ○ ○ ○ ○	
FSM_05		○ ○ ○ ○ ○	1
FSM_06		○ ○ ○ ● ○	2
FSM_07		○ ○ ■ ○ ○	
FSM_08		○ ○ ■ ● ○	/
FSM_09		○ ● ○ ○ ○	/
FSM_10		○ ■ ○ ■ ○	,
FSM_11		● ○ ○ ○ ○	
FSM_12		● ○ ○ ● ○	
FSM_13		● ○ ○ ○ ○	
FSM_14		● ○ ○ ○ ○	
FSM_15	● ○ ○ ○ ○		
FSM_16			
FSM_17		● ■ ■ ■ ■ ●	
FSM_18		● ○ ■ ○ ●	
FSM_19		○ ○ ○ ○ ○	
FSM_20		○ ○ ○ ○ ●	
















LED

RUN, TOKEN, TX/RX, FAULT, SYS FAULT


















Off







7.1.4 (GOL - SMQA/SMIA/SMHA) LED

		LED PWR/ONTX/ERR	
FSM_30		  	
FSM_31		  	
FSM_32		  	
FSM_33		  	
FSM_34	Off	  	Off







7.1.5 (GOL - FREA) LED

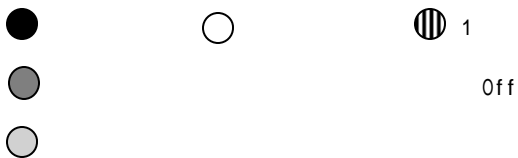
		LED PWR/TRXA/TRXB	
FOU_40		  	
FOU_41		  	A 가
FOU_42		  	B 가
FOU_43		  	
FOU_44	Off	  	Off

7.1.6 (GOL - FOEA) LED

		LED PWR/TRX	
FOU_50		 	
FOU_51		 	가
FOU_52	Off	 	Off

7.1.7 ( ) LED

		LED PWR/TRX	
FOU_60		 	
FOU_61		 	가
FOU_62	Off	 	Off



8

8.1

PLC CPU CPU 가

[ 8.1] CPU 가

CPU	가	가	(Slot)	
GMR	G3L-FUEA, G3L-FUOA	4(2)		2 4 가
GM1/2	G3L-FUEA, G3L-FUOA	4	I/O	
GM3	G3L-FUEA, G3L-FUOA	4	I/O	
K1000S	G3L-RBEA, G3L-RBOA	1	CPU	I/O
GM4	G4L-FUEA, G4L-FUOA	2	I/O	
K300S	G4L-RBEA	1	CPU	I/O
GM6	G6L-FUEA	2	I/O	
K200S	G6L-RBEA	1	CPU	I/O
GM7	G7L-FUEA	1	I/O	
FAM5.0	GOL-FUEA	1	16	PC (ISA BUS)
	GOL-SMQA			Relay
	GOL-SMIA			DC24V
	GOL-SMHA			/
	GOL-FREA			( )
	GOL-FOEA			( )

8.1.1 Fnet

- 1) G3L-FUEA, G4L-FUEA, G6L-FUEA, G7L-FUEA G3L-FUOA, G4L-FUOA, IBM-PC ISA GOL-FUEA 가 . GMR CPU 2 4 가 가 . GM1, GM2, GM3 CPU 4 , 가 . Fnet, Enet(Ethernet) 4 , Cnet( ) 4 .

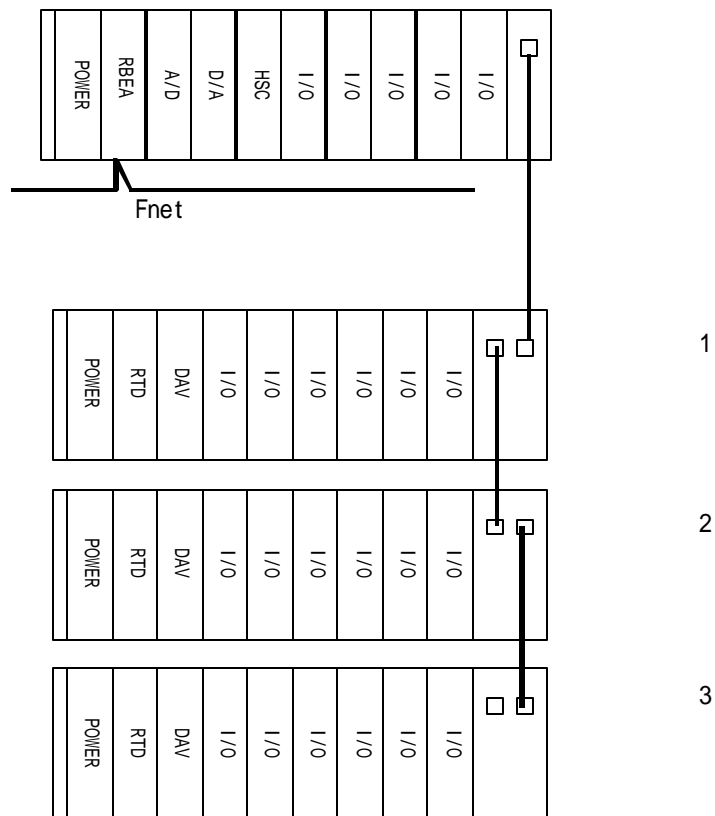
- 2) GM4, GM6 CPU 2 (Enet, Cnet)
  - 3) GM7 CPU 1 (Cnet, Porfibus)
  - 4) GOL-FUEA IBM PC 16 ISA BUS
- (3.2.3 GOL-FUEA).

8.1.2 Fnet

G3L-RBEA, G4L-RBEA, G6L-RBEA G3L-RBOA 16  
 (GOL-SMQA/GOL-SMIA/GOL-SMHA) I/O

[ 8.1.2]

GLOFA GM3/GM4 MASTER- K K1000S/K300S 3 가  
 , GMR/GM1/GM2



[ 8.1.2] GM3/GM4 K1000S/K300S

[ 8.1.2] 가 / 가 ,  
1 /2 /3 .

[ 8.1.2] 가

가	가	
		GM1-CORA
A/D, D/A		G F-INTA
(TC,RTD)	Fnet, Enet, Dnet	G L-FUEA/FUOA G L-EUEA/DUEA
(GLOFA )	PID	G F-PIDA
		G F-AT A
	(MASTER-K )	G L-CUEA G F-HSCA

3,4,6

GLOFA CPU

가 CPU가 MASTER-K  
CPU .

### 8.1.3 Fnet

- 1)
- 2) PLC
- 3)
- 4) 가
- 5) GM1, GM2, GM3, K1000S Fnet 가  
4 (Enet/Dnet , Cnet )
- 6) 가 (Lock) 가 , CPU
- 7)
- 8) CON1 CON2  
( :110Ω)

- 9) . CON1, CON2
- 10) GLOFA GMWIN, MASTER-K LED KGL-WIN ,
- 11) 가 가 .
- 12) .(4.3.2 ) 가
- 13) PC IBM 가 ISA ,
- 가 . (3.2.3 GOL-FUEA ) .
- 13) PC

8.1.4 Fnet

1)

2)

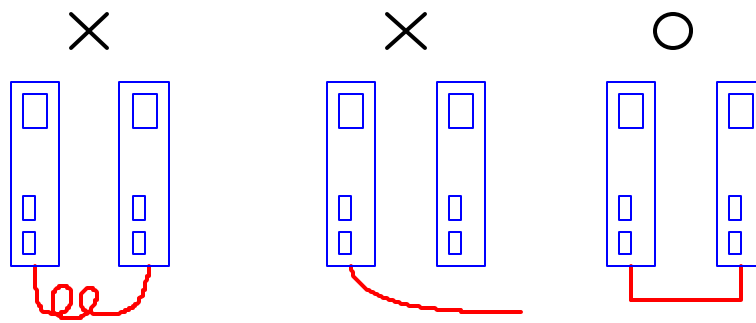
Run

3)

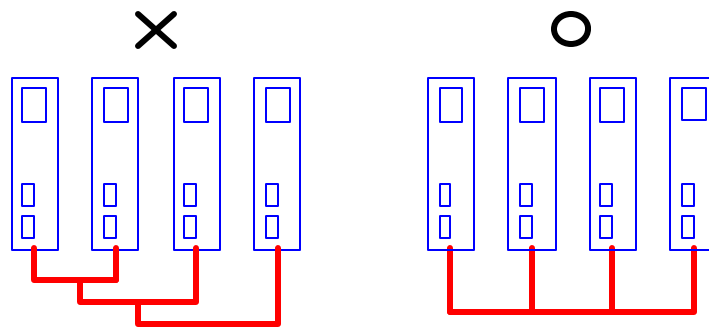
4)

5)

6)

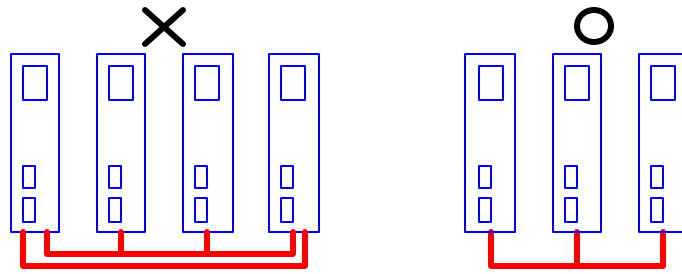


7)





8) 가



9)

10) ( ) 9

(4.4.1 ( ) ).

11)

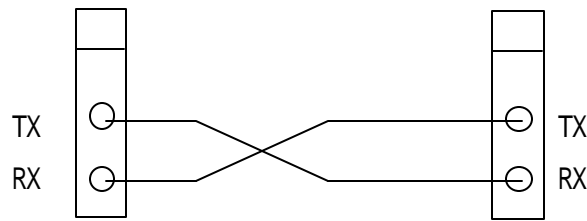
TX RX

TX/RX

TX/RX

가

(4.4.3 ).



12) LED

9

A/S

8.1.5 Fnet

Fnet

1) PLC

	- 가?
	- CPU 가?
	- 가?
	( PLC .)
	- 가?
	- 가?
	- 가?
	- On-Line( 0) 가?
	- 가?
	- 가? ( )
	- 가?
	( )

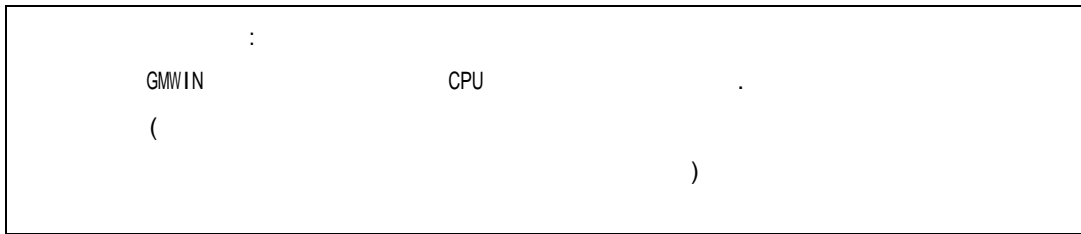
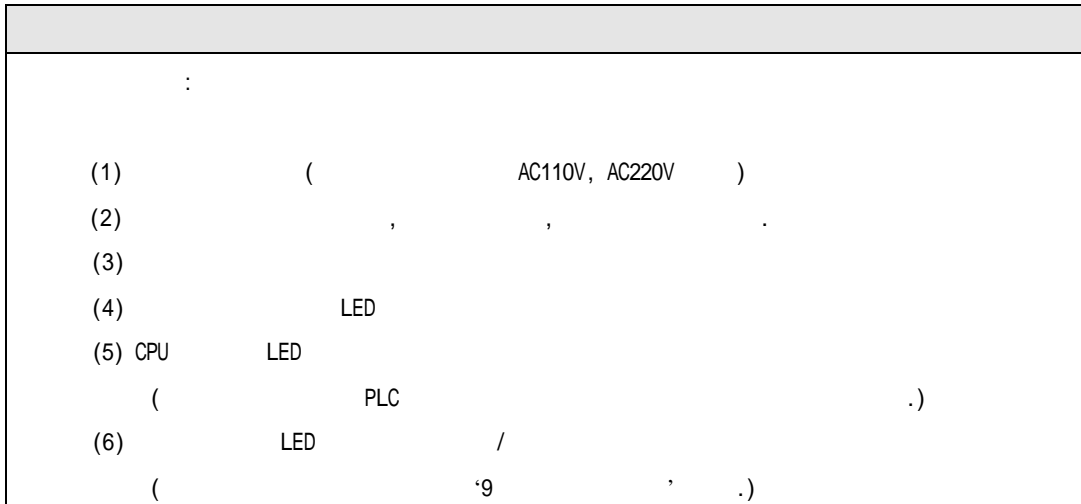
2) PC

	- PC 가 IBM-PC , 16 ISA 가?
	- PC 가 FAM5.0/GMWIN/KGL-WIN 가?
	- PC 가?
	- PC 가?
	(FAM5.0/GMWIN/KGL-WIN ' ' )
FAM4.0/GMWIN	- PC 32k , .
	- 가?
	- 가?

8.1.6 Fnet

PLC

1) PLC



2) PC

	:
(1)	( :AC110V, AC220V)
(2)	,
(3)	
(4) PC	
	( FAM5.0/GMWIN/KGL-WIN ‘ ’ )
(5) LED	,
	( ‘9 ’ )
(6) FAM5.0/GMWIN/KGL-WIN	가
	(FAM5.0/GMWIN/KGL-WIN )
(7) LED	( ‘ LED ’ ,
	‘9 ’ )
(8)	
	(FAM5.0/GMWIN/KGL-WIN .
	‘9 ’ )

(1) FAM5.0/GMWIN/KGL-WIN	.
(2) LED	

8.2

8.2.1

1) Fnet

[ 8.4.1(A)]

LED	RUN LED		( CPU )	
	LAS LED		LED가 ( )	
	TOKEN LED		( )	
	TX/RX LED		( )	
	FAULT LED			

2) Fnet

[ 8.4.1(B)]

LED	RUN LED			
	TOKEN LED		.( )	
	TX/RX LED		( )	
	FAULT LED		( )	
	SYS FAULT LED		(LED )	

8.2.2 : 6 1~2

[ 8.4.2]

		/	0 ~ 55	(
			5 ~ 95%RH	
		가	가 가	
	,	.		
	,			
			AC 85 ~ 132V AC 170 ~ 264V	

9

가 LED  
 LED ( :FMM\_06),  
 ( :E00-01)

9.1

[ 9.1(A)]

	( LED )	
E00-01	FMM_06 ~ FMM_10 FMM_24 ~ FMM_27 FSM_05 ~ FSM_10 FSM_32 MCM_06 ~ MCM_09	LED
E00-02	FMM_11 ~ FMM_13 MCM_11	LED PLC
E00-03	FOU_41, FOU_42, FOU_43, FOU_44 FOU_51, FOU_52, FOU_61, FOU_62	FOU
E00-04	FSM_08 ~ FSM_10	/ ,

[ 9.1(B)]

E01-01	FMM_16 ~ FMM_21 FSM_13 ~ FSM_16 FSM_31, FSM_33	Fnet ( )
E01-03	FOU_41, FOU_42, FOU_43 FOU_51, FOU_61	Fnet FOU ( )

[ 9.1(C)] PLC

E02-01	FMM_22, FMM_23 MCM_11	가 PLC
E02-02	FSM_08 ~ FSM_10	Fnet

[ 9.1(D) ]

E03-01		가 ,      가
E03-02		가
E03-03	_HSxTRX      _HSxRLNK, On	가      _HSxRLNK 가 On
E03-04	On      _HSxLTRBL	_HSxRLNK 가 On PLC HSxLTRBL    On

[ 9.1(E) ]

E04-01	Fnet      가 ERR      On STATUS      0	ERR 가 On NDR/ERR    1
--------	---	--------------------------

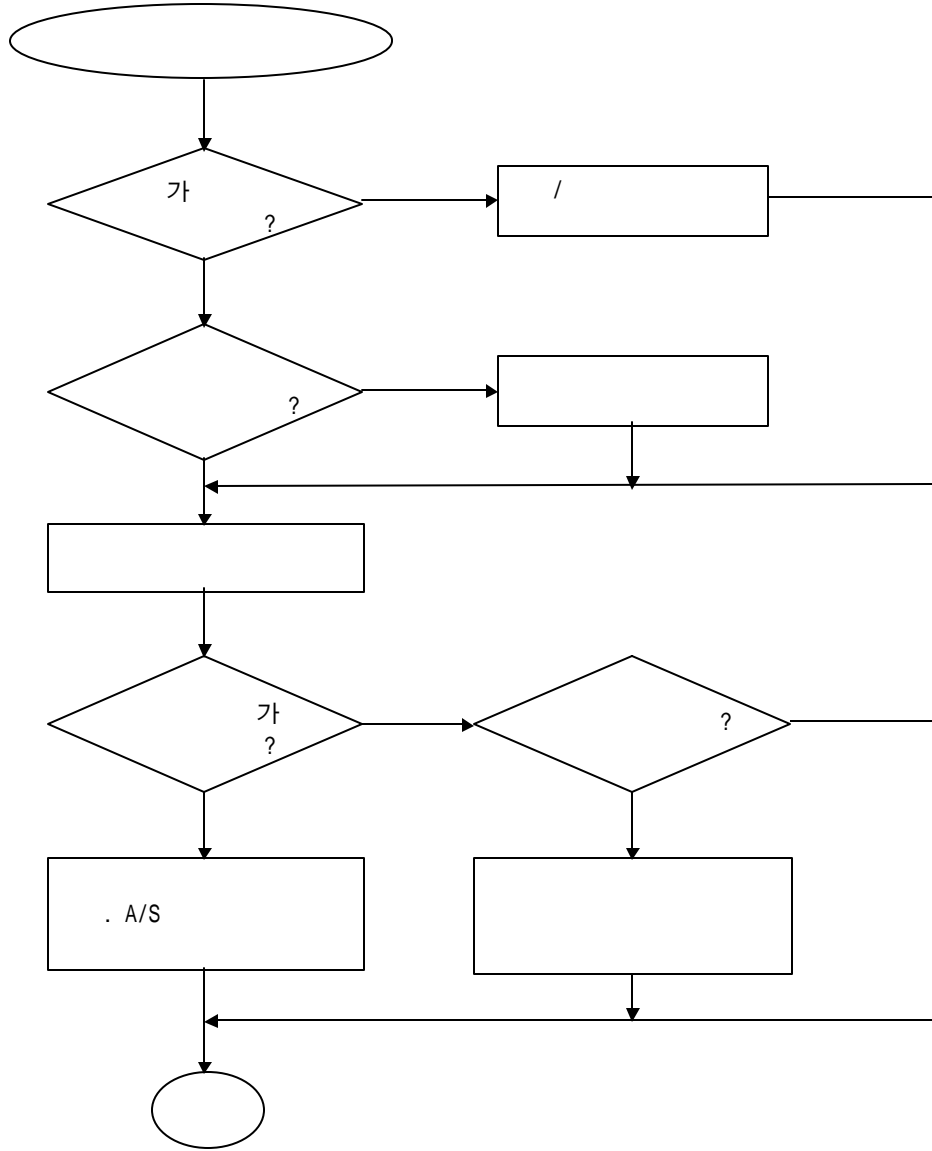
[ 9.1(F) ] GMWIN

E05-01	[                      ]	GMWIN    PLC      RS-232C PLC      Off
E05-02	가	가

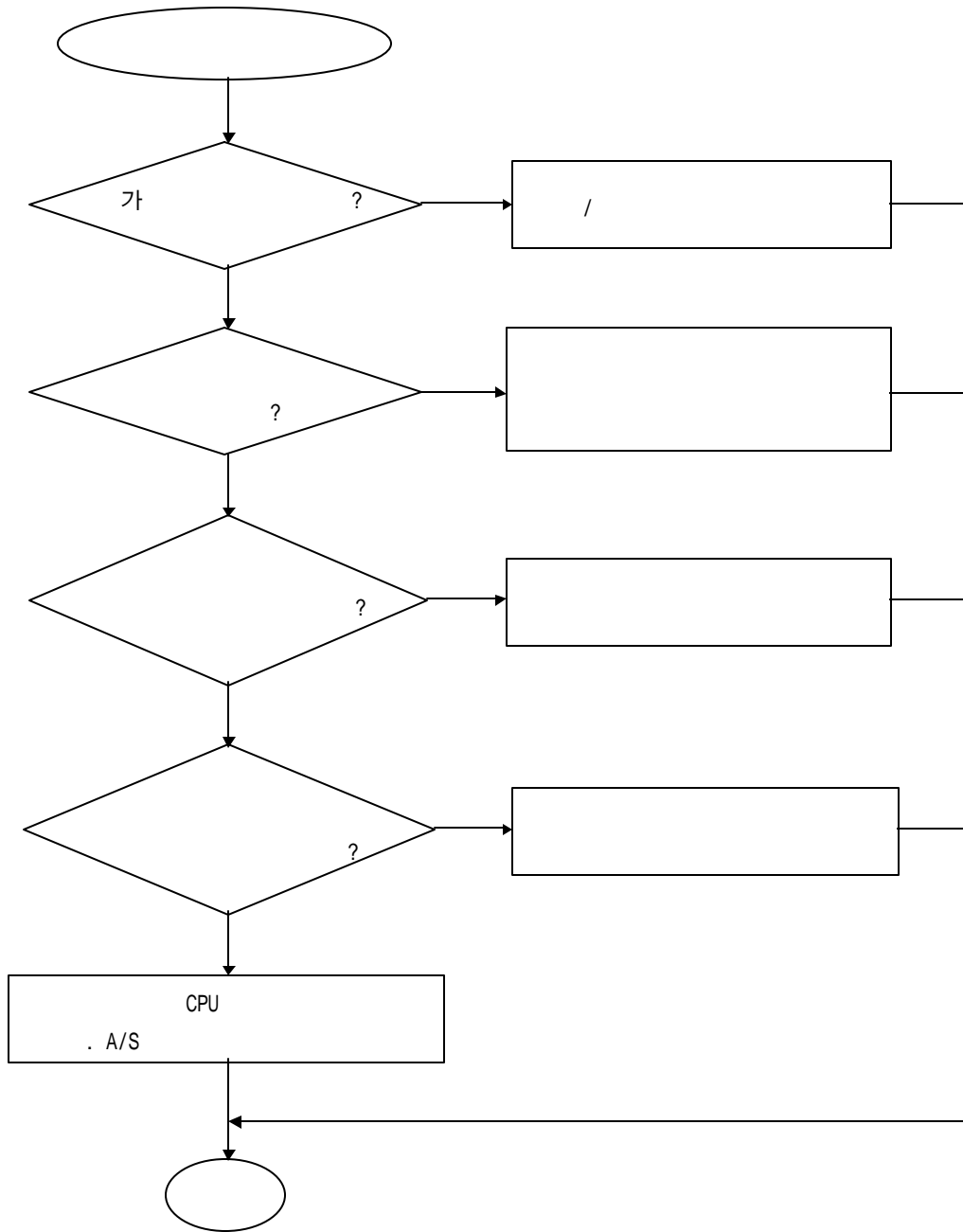


9.2

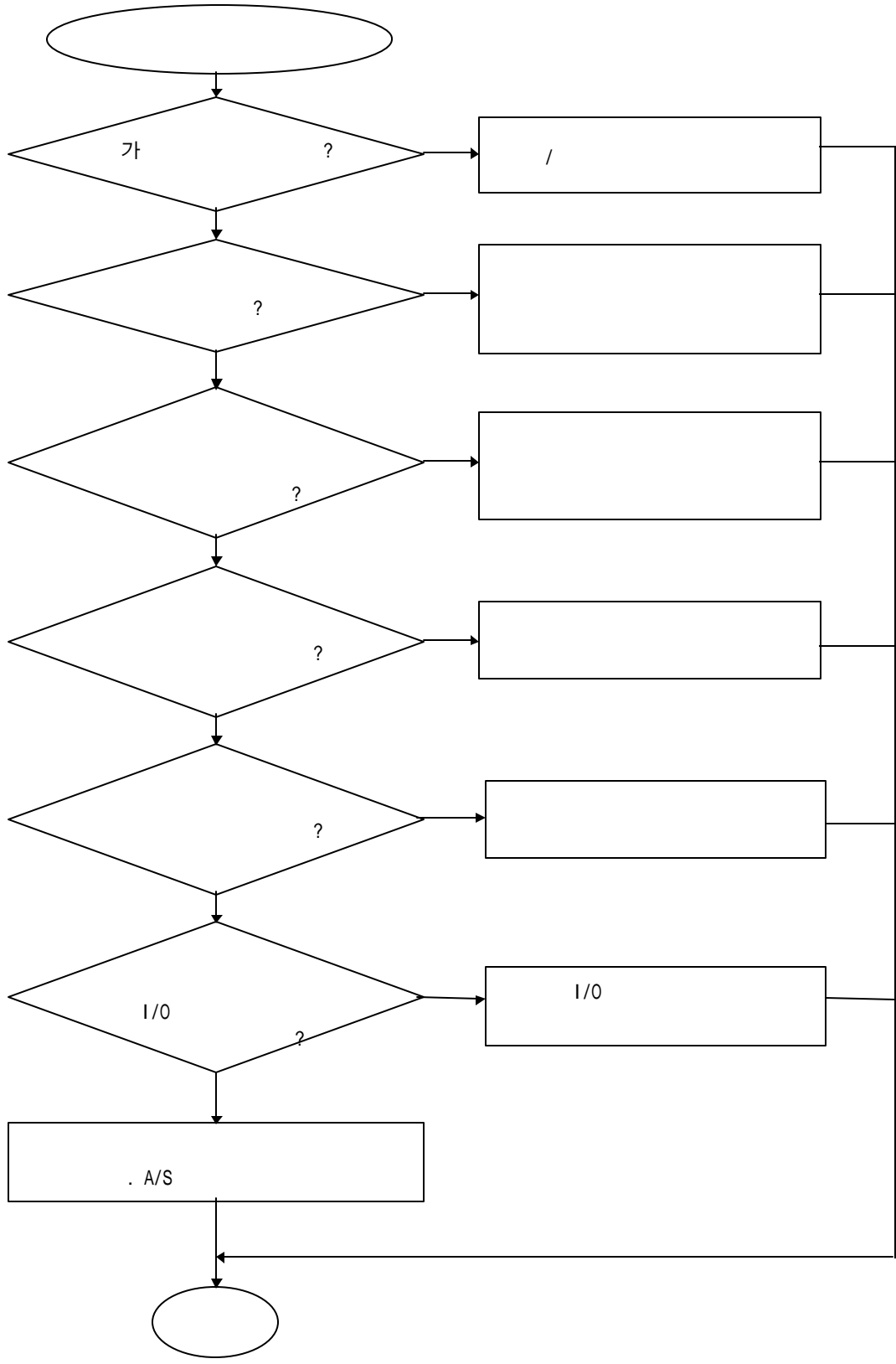
9.2.1 E00-01 :  
E00-03 :



9.2.2 E00-02 :



9.2.3 E00-04:FSM(Fieldbus Slave Module)

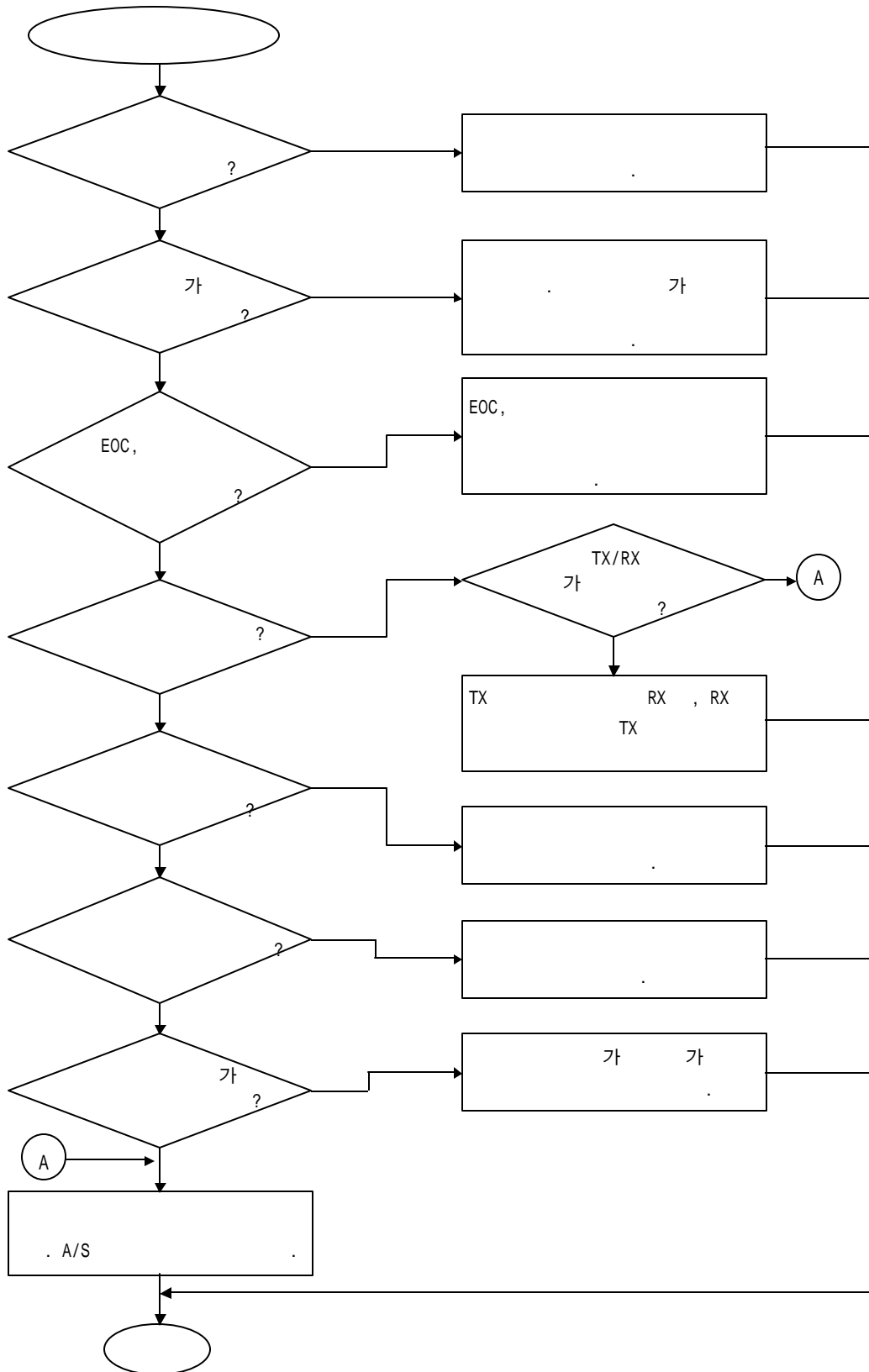




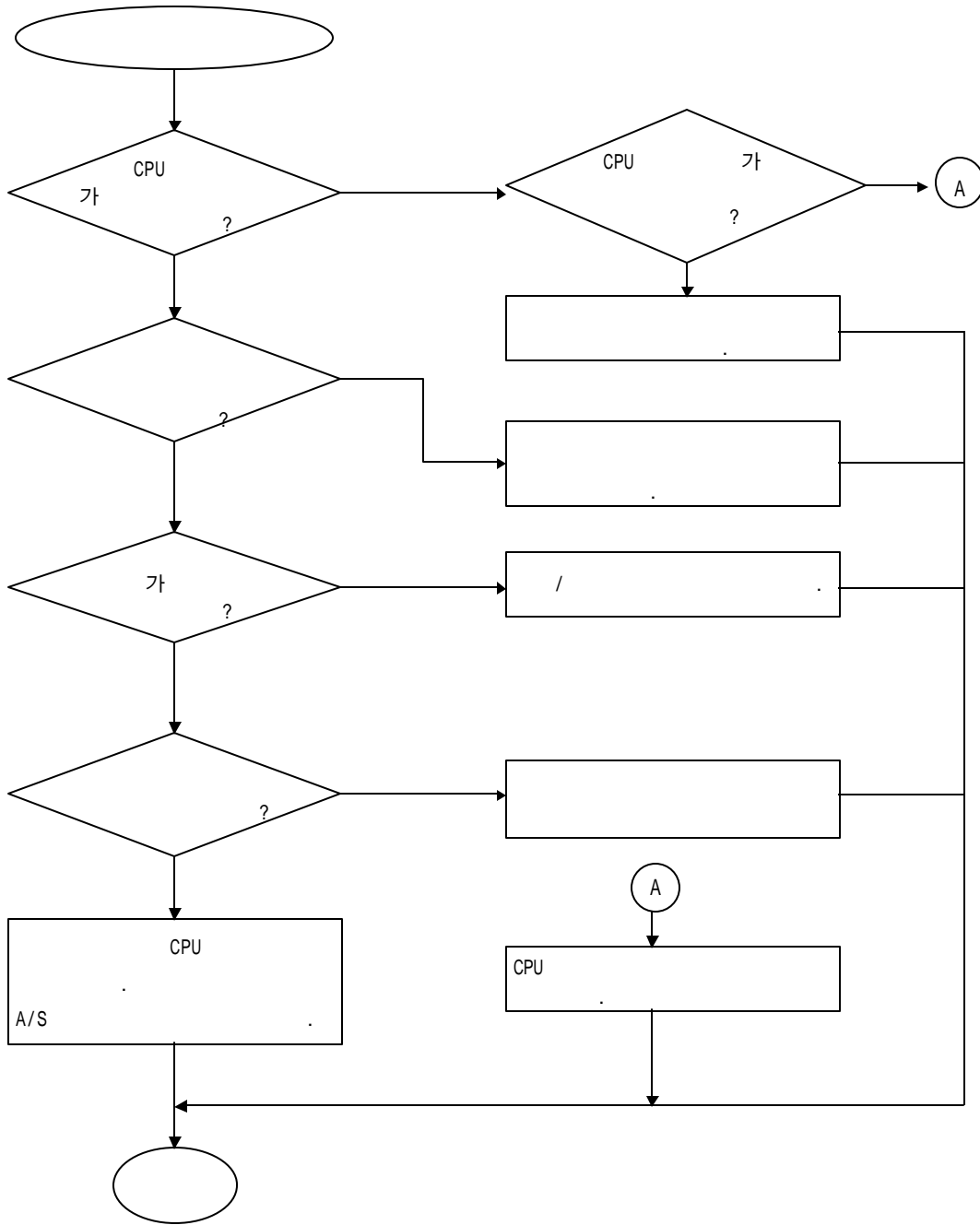
9.2.4

E01-01:Fnet

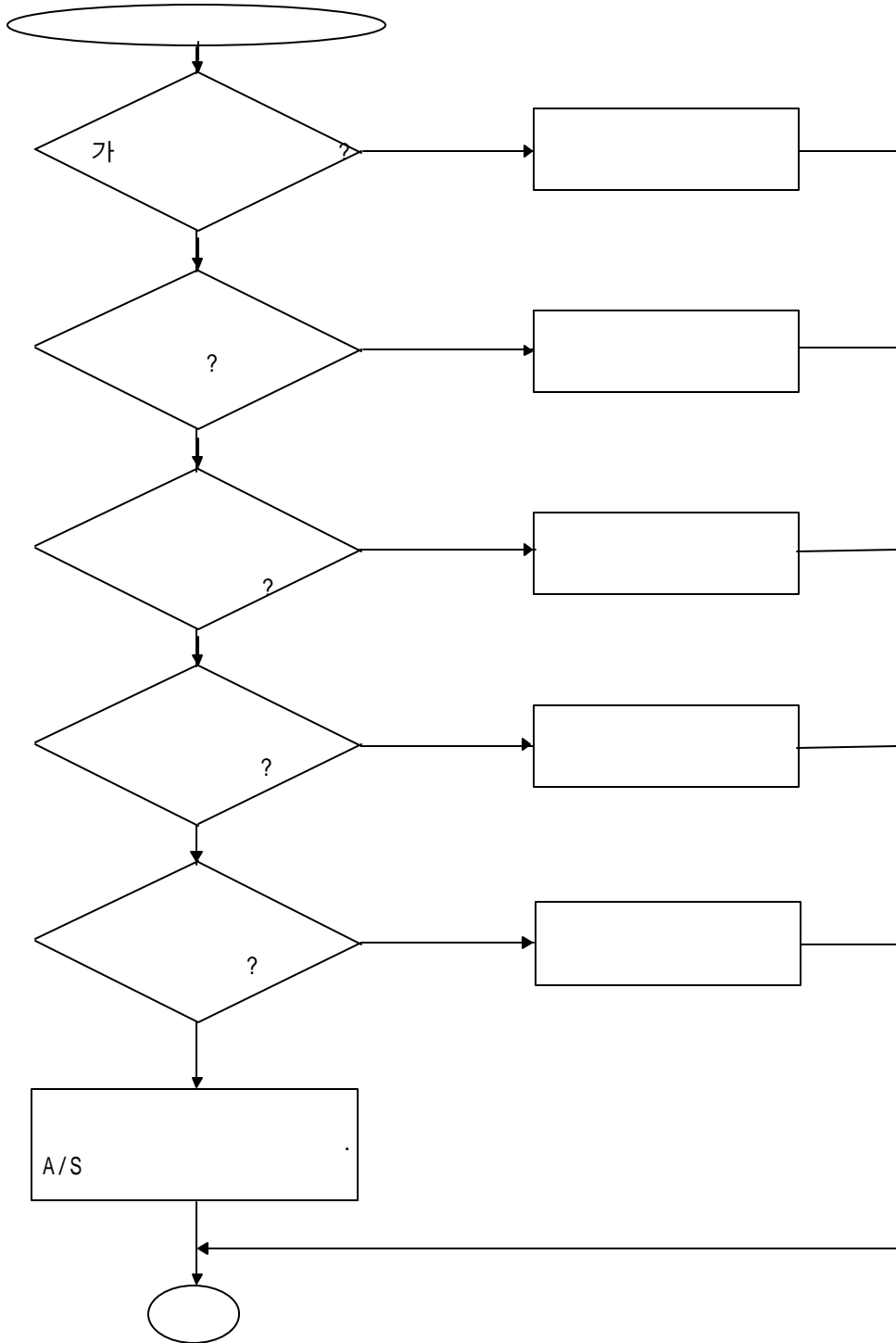
, E01-03:FOU



9.2.5 E02-01 : PLC

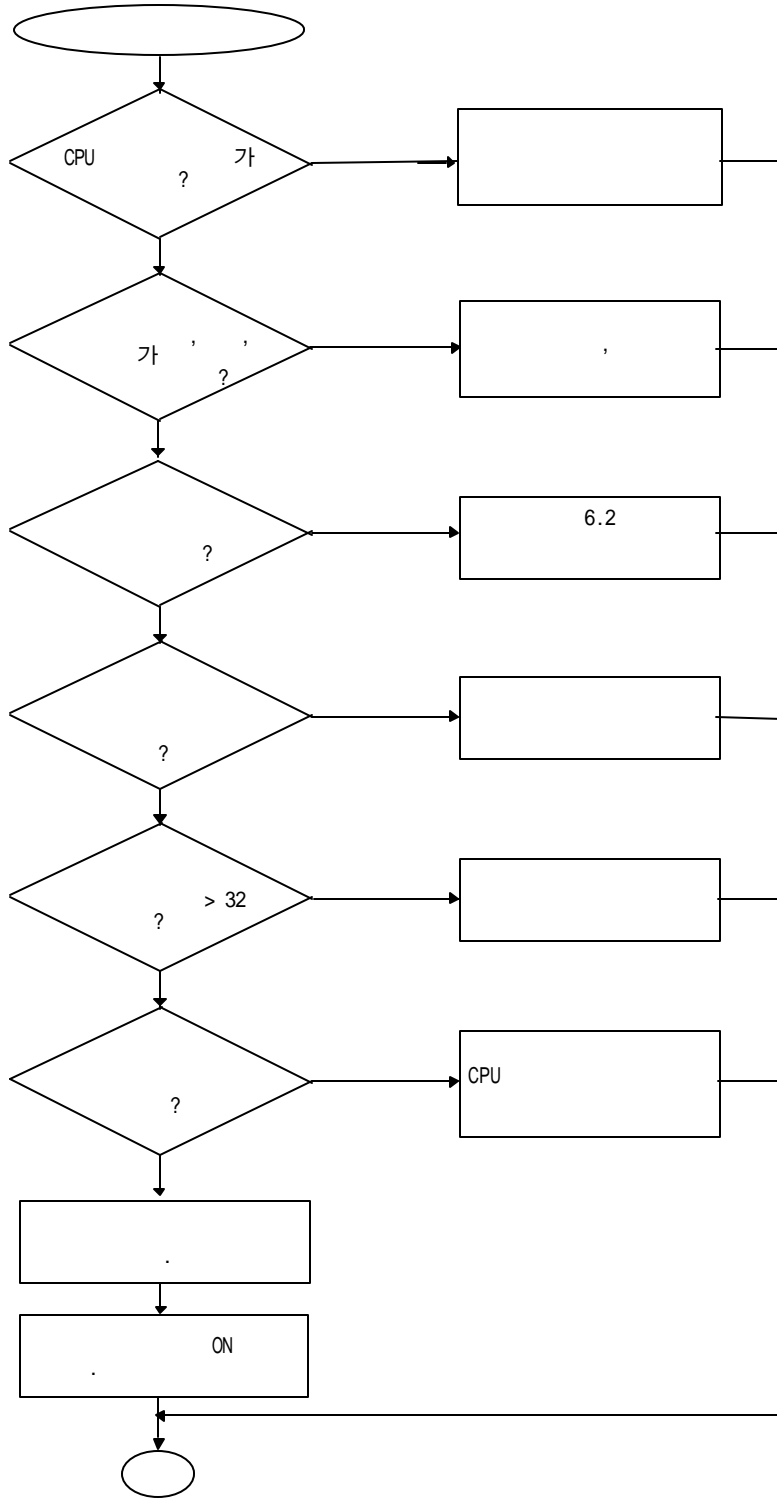


9.2.6 E02-02 :



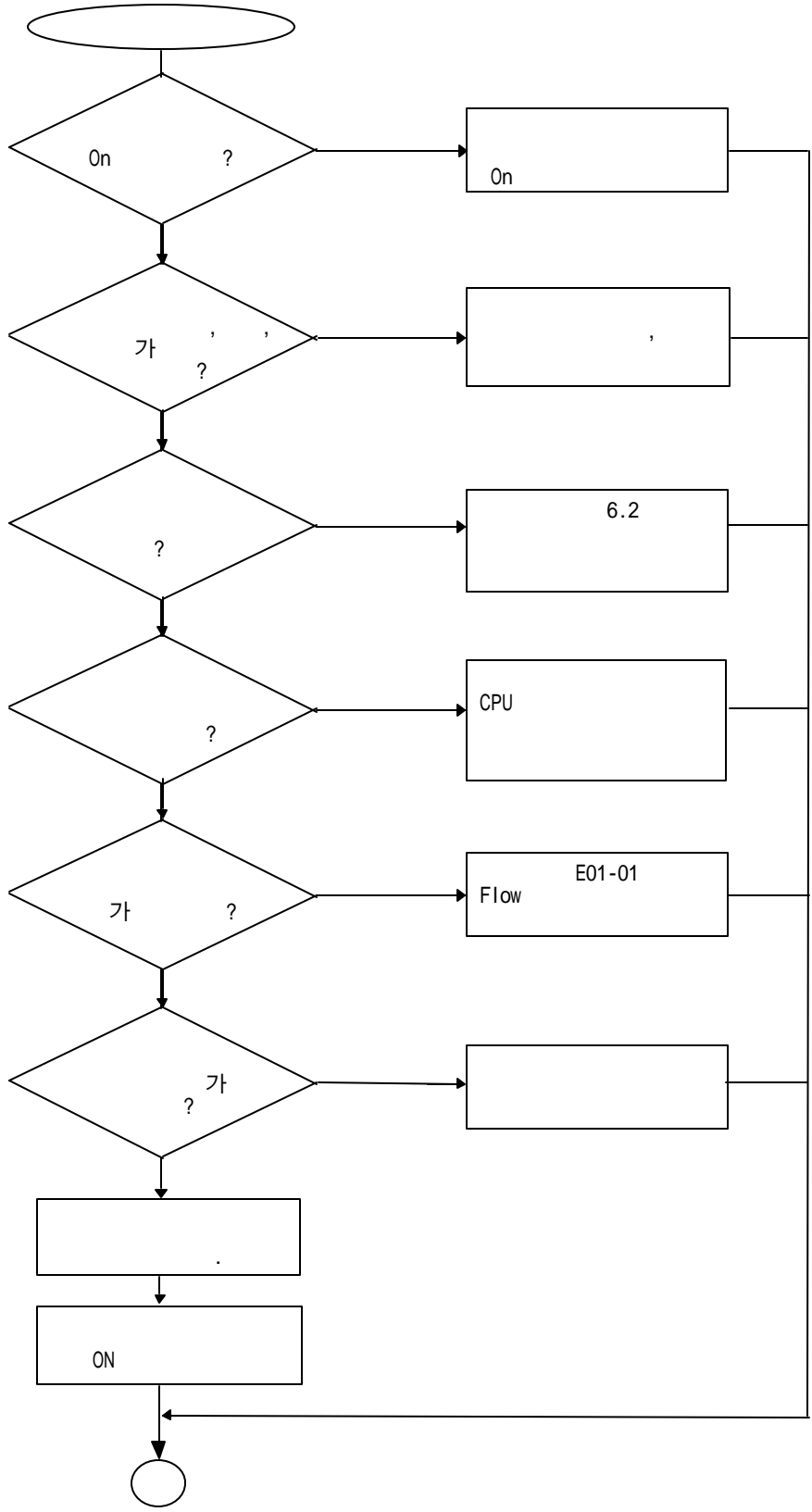
9.2.7

E03-01 :





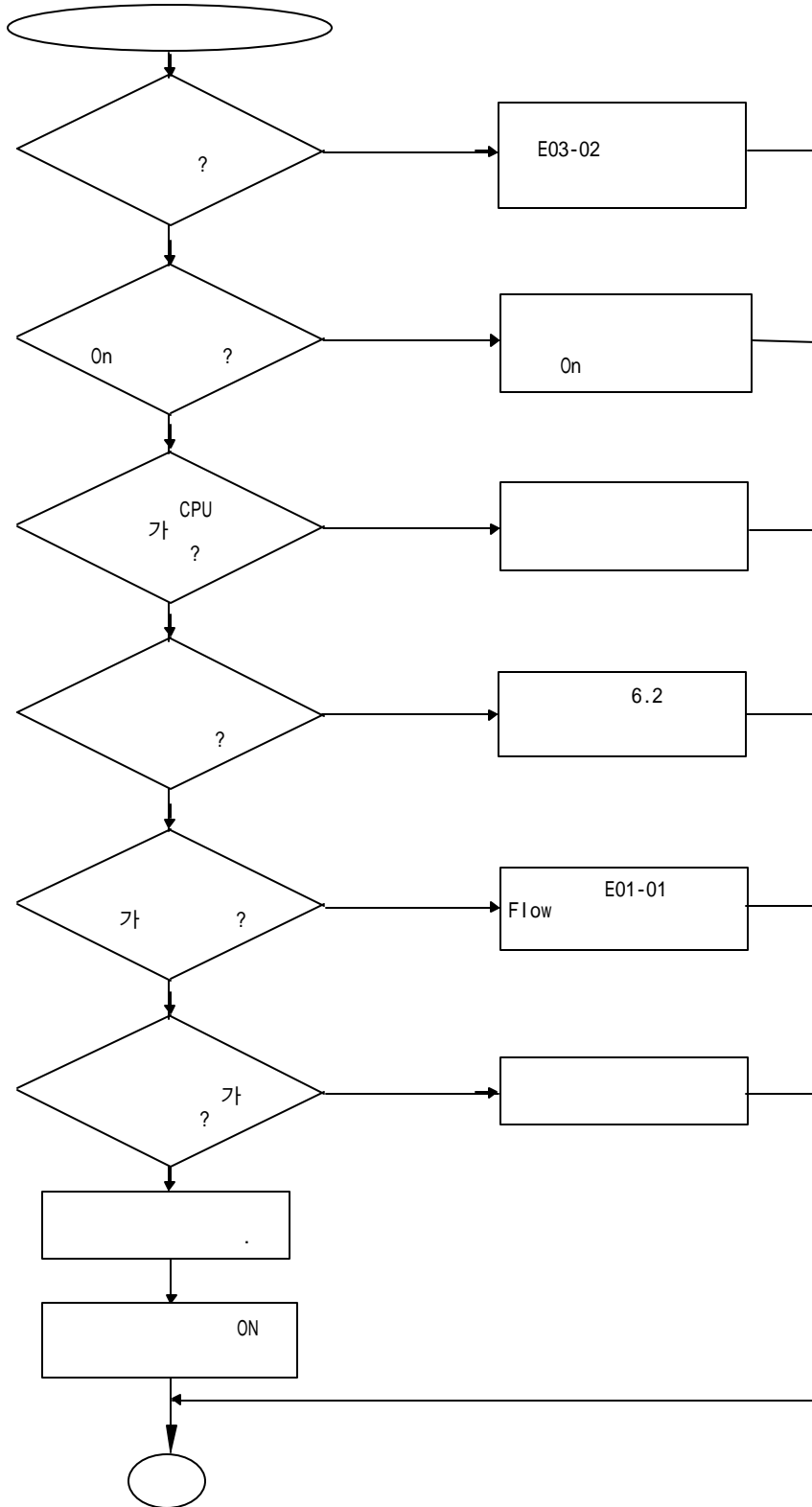
9.2.8 E03-02 :



9.2.9

E03-03 :

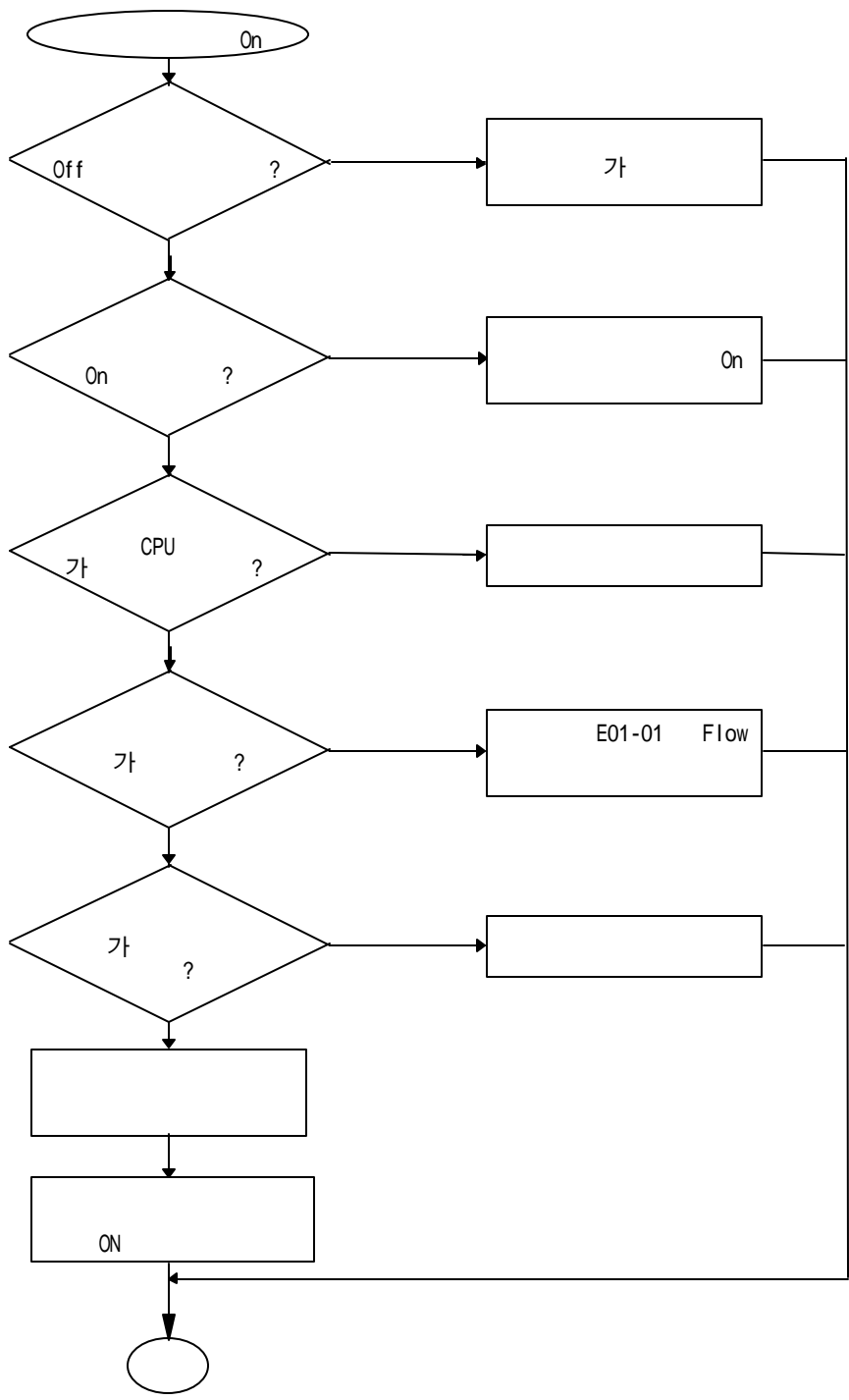
0n



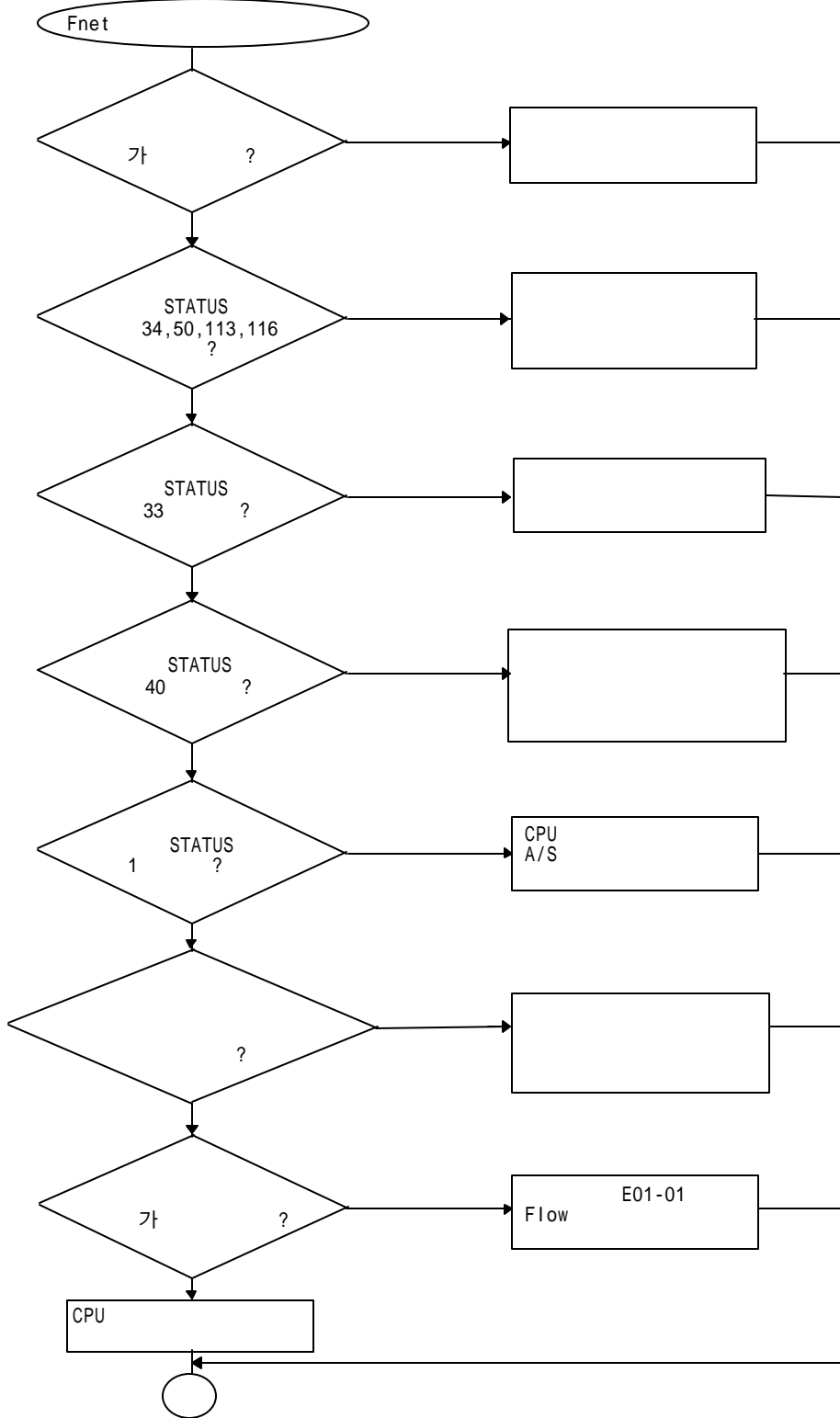
9.2.10

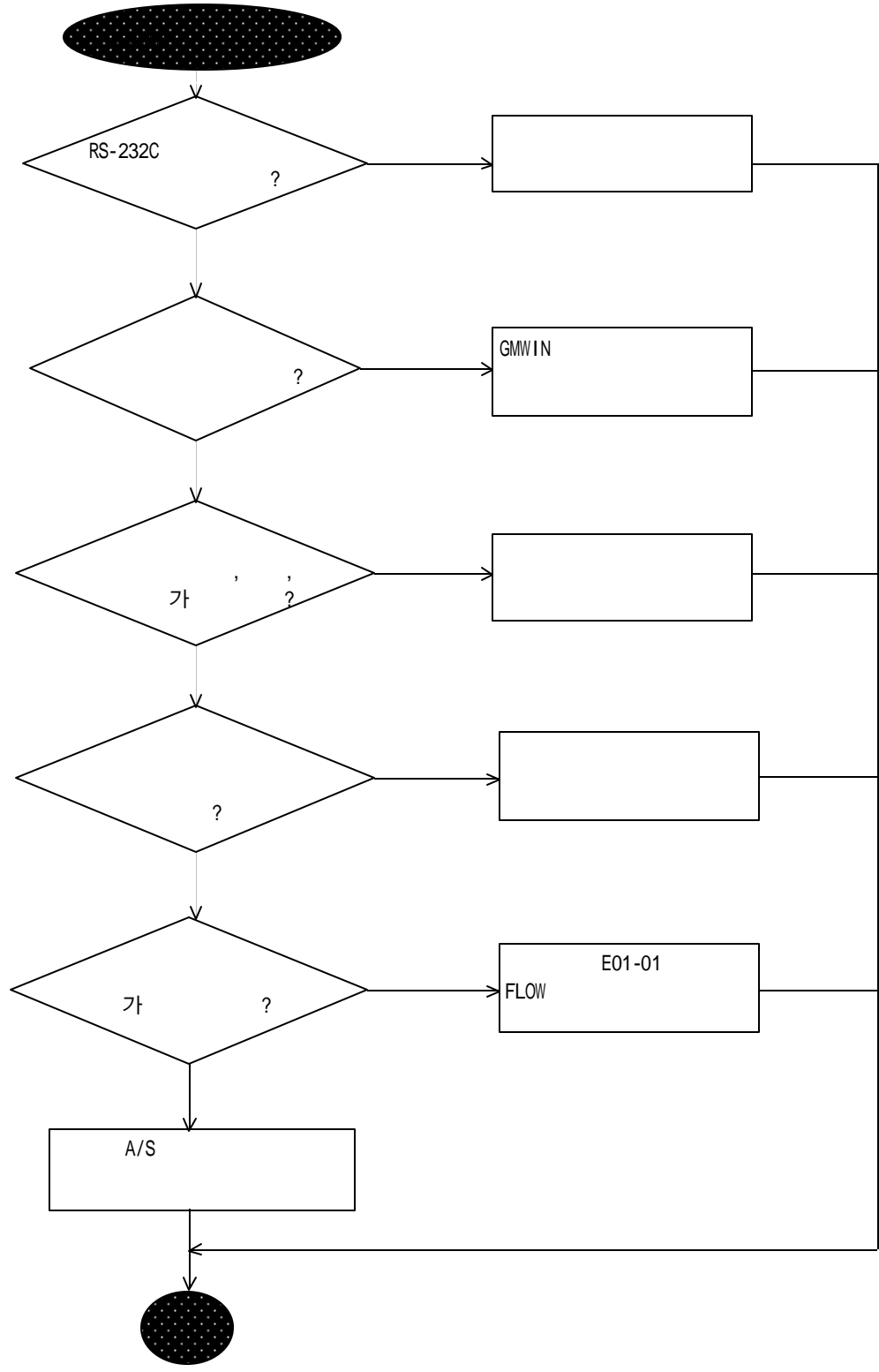
E03-04 :

On

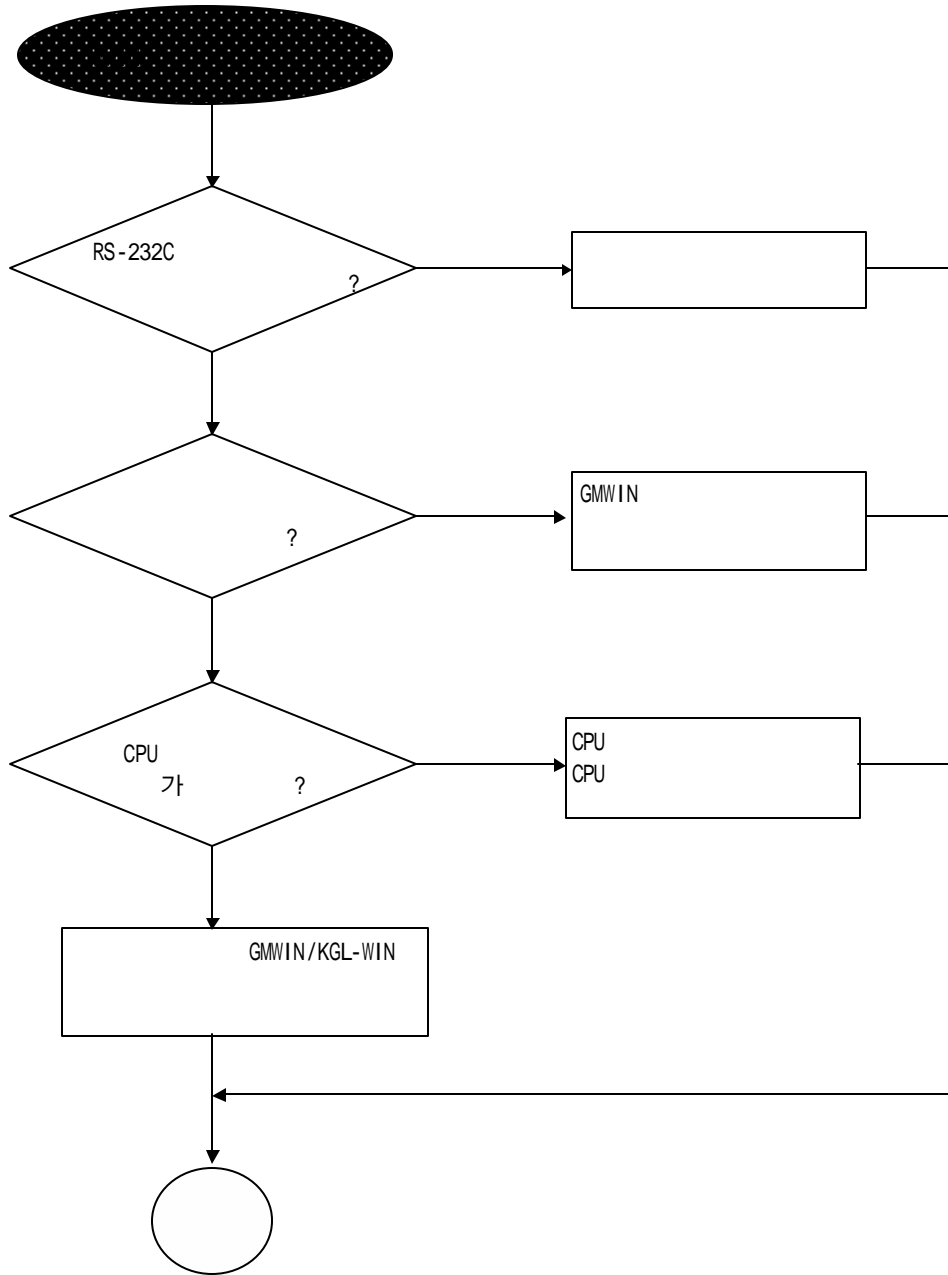


9.2.11 E04-01 : Fnet





9.2.13 E05-02 : Fnet GMWIN



**A1 PC Fnet (GOL-FUEA)**

- 1) : GOL-FUEA
- 2) : PC Fnet (GOL-FUEA) 32kByte I/O PC

I/O ( ) 32 , 16k  
 [ A1.1] /

(HEX)	I/O	Fnet (GOL-FUEA)	
0	3E0	FC00	* I/O 5 (340), D (C800)
1	3C0	F800	
2	3A0	F400	
3	380	F000	
4	360	EC00	
5	340 *	E800	
6	320	E400	
7	300	E000	
8	2E0	DC00	
9	2C0	D800	
A	2A0	D400	
B	280	D000	
C	260	CC00	
D	240	C800 *	
E	220	C400	
F	200	C000	

1) I/O 가 PC 가

2) C800 - DBFF

2) CONFIG.SYS DEVICE=C:\WINDOWS\EMM386.EXE NOEMS X=C800-DBFF  
 [ D (C800) ]

A2 (GLOFA) / (MK) STATUS

A2.1

GLOFA (10 )	MK (16 )	
0	H00	( )
1	H01	( , 가) - Off, .
3	H03	가 . ( )
4	H04	
5	H05	( )
6	H06	가 가 ( )
7	H07	가 가 ( )
8	H08	가 가 가
9	H09	가 가 ( )
10	H0A	(Time Out) - .
11	H0B	Structure
12	H0C	Abort( / ) :
13	H0D	Reject( / ) - MMS .
15	H0F	
33	-	:
34	H22	- Structure (Range)
50	H23	: CPU
113	H71	Object Access Unsupported - VMD Specific Symbolic Address
187	HBB	( ) - .



A2.2 CPU

STATUS

1)

GLOFA (10 )	MK (16 )	
16	H10	
17	H11	SLOT_NO
18	H12	
19	H13	
20	H14	
21	H15	( -Time Out)

2)

(FSM)

STATUS

GLOFA (10 )	MK (16 )	
128	H80	FSM
129	H81	BASE(Rack)
130	H82	
131	H83	
132	H84	(Invalid Range)
133	H85	
136	H88	( )
137	H89	

A 3

A 3.1 ( )

[ A3.1] Fnet KGL-WIN

[ A3.1] (0 ) x:K1000S=9, K300S/K200S=4, n:0~7( )

		Type	
Dx500 Dx502	_CnSTNOL _CnSTNOH	DWord	
Dx504	_CnTXECNT	Word	1 가 가
Dx505	_CnRXECNT	Word	1 가 가
Dx506	_CnSVCFCNT	Word	1 가 가 가
Dx507	_CnSCANMX	Word	(1ms ) TOKEN
Dx508	_CnSCANAV	Word	(1ms ) TOKEN
Dx509	_CnSCANMN	Word	(1ms ) TOKEN
Dx510	_CnLINF	Word	
Dx510.0	_CnCRDER	Bit	( =1) H/W O/S
Dx510.1	_CnSVBSY	Bit	( =1) 가
Dx510.2	_CnIFERR	Bit	( =1) 가
Dx510.3	_CnINRING	Bit	(가 =1) 가
Dx510.4	_CnLNKMOD	Bit	( =1) 가 TEST
Dx680	_CnVERNO	Word	No. O/S No.
Dx690	_FSMn_st_no	Word	I/O 8bit I/O ( )
Dx690.0	_FSMn_reset	Bit	I/O s/w reset _FSMn_st_no I/O
Dx690.1	_FSMn_io_reset	Bit	I/O reset _FSMn_st_no I/O
Dx690.2	_FSMn_hs_reset	Bit	I/O _FSMn_st_no bit off bit ON bit가 ON 1 , 0

[ A3.2]

	D	
1	Dx511 ~ Dx521	[ A4.1] 0 가 n
2	Dx522 ~ Dx532	
3	Dx533 ~ Dx543	
4	Dx544 ~ Dx554	: n=1~7 D = [ A4.1] + 11 ' n
5	Dx555 ~ Dx565	

6	Dx566 ~ Dx576	) 6 = Dx508+11×6 = Dx574
7	Dx577 ~ Dx587	

1) Dx680, Dx690	8bit	가	Dx680 ~ Dx687	0	7	
	O/S	가	I/O	Dx690 ~ Dx697	0	7
		I/O				
2) _FSM3_st_no(Dx693)	8bit	h10	3		16	
	_FSMn_reset, _FSMn_io_reset, _FSMn_hs_rese			, hFF	3	

[ A3.3] L (0) x : , n :

_NETx_LIV[n]	L0000 ~ L003F	L0000 ~ L000F(0~15 )	Alive , 가 ( 가 )
		L0010 ~ L001F(16~31 )	
		L0020 ~ L002F(32~47 )	
		L0030 ~ L003F(48~63 )	
_NETx_RST[n]	L0040 ~ L07F	L0040 ~ L004F(0~15 )	"On" ( / 가 )
		L0050 ~ L005F(16~31 )	
		L0060 ~ L006F(32~47 )	
		L0070 ~ L007F(48~63 )	

1) n 0 ~ 63 , x  
가 x 0 8x L

1	L0080 ~ L015F	* 8 Reset Alive , 4
2	L0160 ~ L023F	
3	L0240 ~ L031F	
4	L0320 ~ L039F	
5	L0400 ~ L047F	
6	L0480 ~ L055F	
7	L0560 ~ L063F	

2) L 가  
L 가

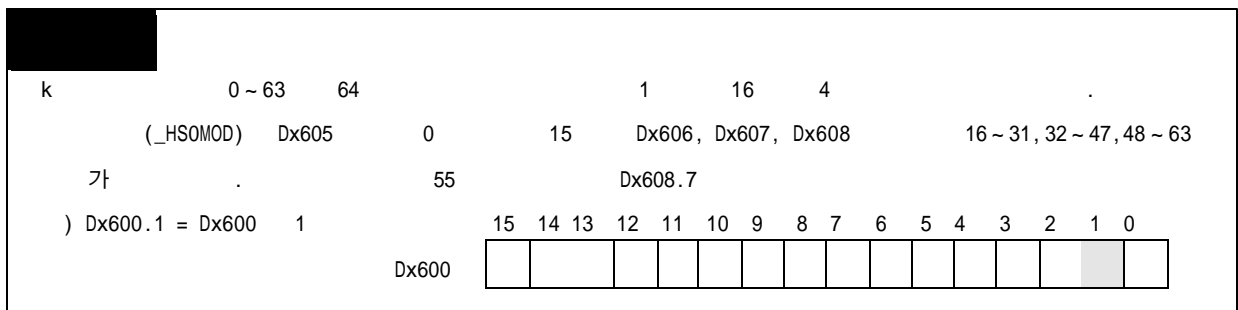
A3.2

[ A3.4] x : K1000S=9, K300S/K200S=4 m :

	Type	Bit		
_HSmRLINK	Bit	Dx600.0	RUN_LINK	1. RUN 가 2. 가 3. 가 - ON ON
_HSmLTRBL	Bit	Dx600.1	(LINK_TROUBLE)	_HSmRLINK가 ON 가 ON 1. RUN 가 2. 가 3. 가 1,2,3 가 OFF ON ,
_HSmSTATE[k] (k=0 ~ 63)	Bit Array	Dx601.0 ~ Dx604.15	k	_HSmSTATE[k] = _HSmMOD[k] & _HSmTRX[k] & _HSmERR[k]
_HSmMOD[k] (k=0 ~ 63)	Bit Array	Dx605.0 ~ Dx608.15	(RUN = 1, = 0)	k
_HSmTRX[k] (k=0 ~ 63)	Bit Array	Dx609.0 ~ Dx612.15	( =1, =0)	k 가
_HSmERR[k] (k=0 ~ 63)	Bit Array	Dx613.0 ~ Dx616.15	k ( =1, =0)	k 가

[ A3.5] m=1 ~ 3

	D	
High Speed Link2 (m=1)	Dx620 ~ Dx633	[ A4.3] m=0 m=1 ~ 3 D
High Speed Link3 (m=2)	Dx640 ~ Dx653	.
High Speed Link4 (m=3)	Dx660 ~ Dx673	: m=1 ~ 3 D = [ A3.3] + 20 ~ m



A3.3

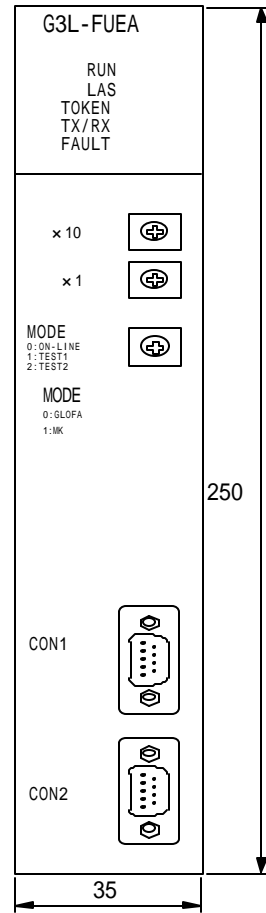
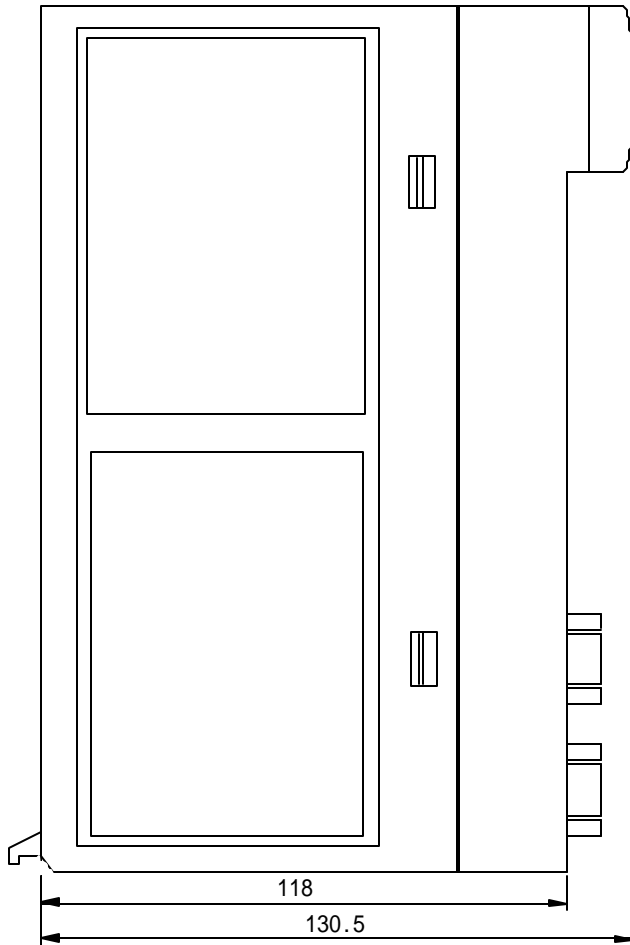
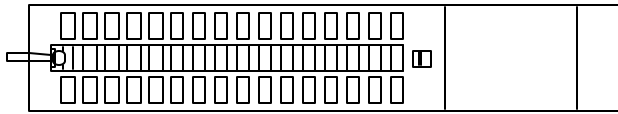
[ A3.6]

Key Word		( 16 )			
_CPU_Type	CPU Type	h0000	Word	2 Byte	
_VER_NUM	O/S Version Number	h0002	Word	2 Byte	
_SYS_STATE		h0004	Word	2 Byte	
_FSMTXECNT	TX	h0006	Word	2 Byte	
_FSMRXECNT	RX	h0008	Word	2 Byte	
_FSMSVFCNT		h000A	Word	2 Byte	
_FSMScanMX		h000C	Word	2 Byte	
_FSMScanAV		h000E	Word	2 Byte	
_FSMScanMI		h0010	Word	2 Byte	
_MOTHSTNO		h0012	Word	2 Byte	
_FSMVRCNT	RD	h0014	Word	2 Byte	
_FSMVWCNT	WR	h0016	Word	2 Byte	
_FSMHSTXCNT	TX	h0018	Word	2 Byte	
_FSMHSRXCNT	RX	h001A	Word	2 Byte	
_AC_Fail_CNT	Power Fail	h001C	Word	2 Byte	Byte (d7 ~ d15 Byte)
_CNF_ER	CPU	h001E	Word	2 Byte	
d0 : _CPU_ER	I/O I/P SUB POWER		Byte 0		
d1 : _IO_TYER			Byte 1		
d2 : _IO_DEER			Byte 2		
d3 : _FUSE_ER			Byte 3		
d4 : _IO_RWER			Byte 4		
d5 : _IP_IFER		Byte 5			
d6 : _PWR_ERR			Byte 6		
_IO_TYER_N	I/O	h0020	Word	2 Byte	
_IO_DEER_N		h0022	Word	2 Byte	
_FUSE_ER_N		h0024	Word	2 Byte	
_IO_RWER_N		h0026	Word	2 Byte	
_IP_IFER_N		h0028	Word	2 Byte	
_KGL_CNF	KGL-WIN	h002A	Byte	1 Byte	
d0 : local					
d1 : remote					
_E_DATA_OPTION		h002B	Byte	1 Byte	0 : 1 :

A 4

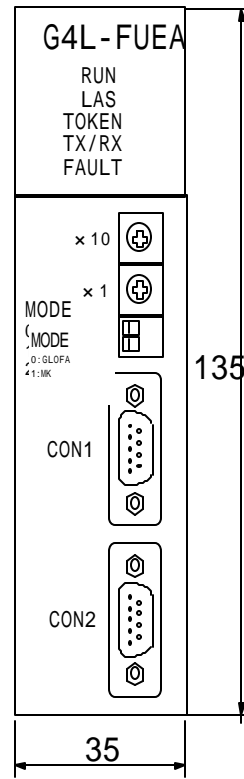
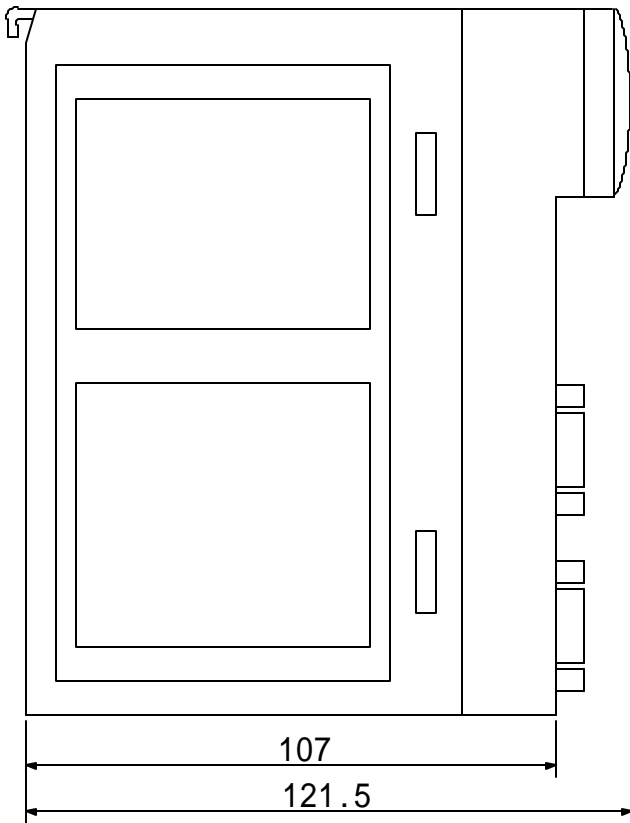
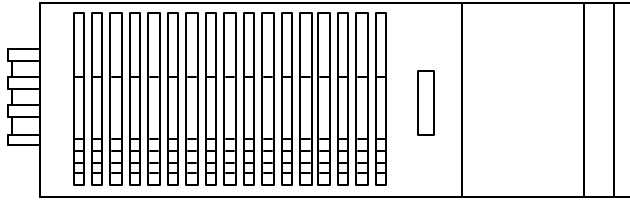
A4.1 GM1/2/3

: G3L-FUEA/FU0A, G3L-RBEA/RB0A



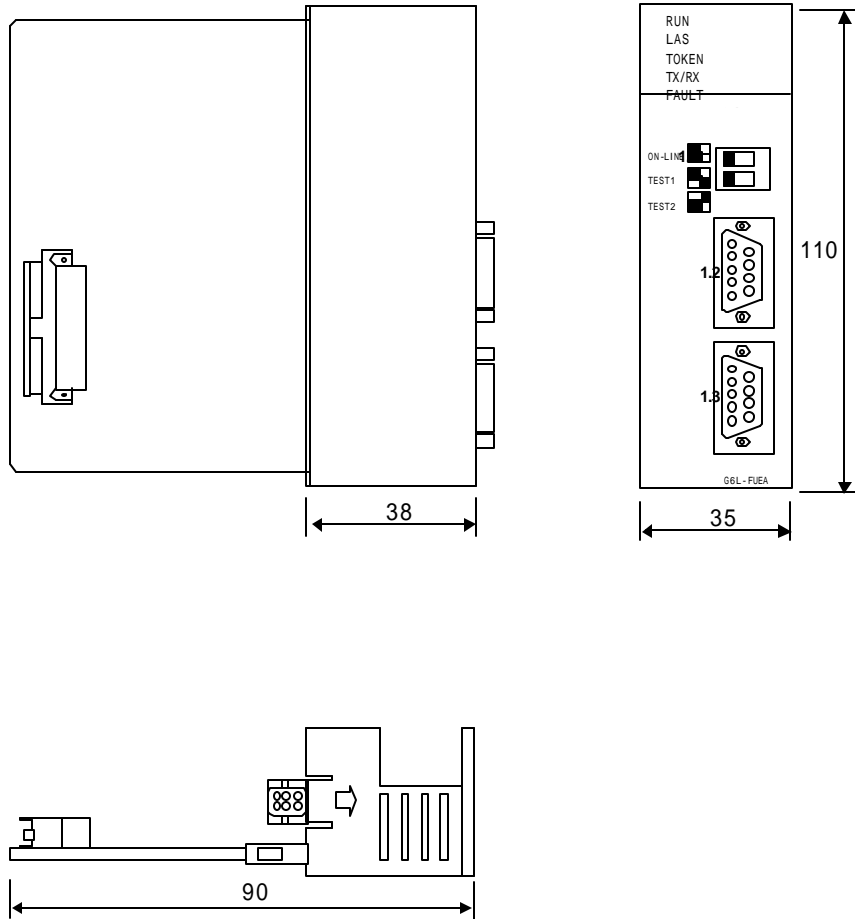
A4.2 GM4

: G4L-FUEA/FU0A, G4L-RBEA



A4.3 GM6

: G6L-FUEA, G6L-RBEA







A4.5 PC( )

: GOL-FUEA

